ELECTRONICS FOR MEASUREMENT • COMPUTATION • TELEMETRY • CONTROL

INSTRUCTION MANUAL

for

PCM SYSTEM

MODEL 4001

DCS DATA-CONTROL SYSTEMS INC.

Instrumentation for Research

East Liberty St., Danbury, Conn. 06810 Telephone: 203-743-9241 TWX 710-456-2596

DIFFERENCE DATA SHEET

INSTRUCTION MANUAL, MODEL 4001

4001-000-006 versus 4001

The 006 modification to the 4001-000 creates the following basic differences between it and a standard unit.

Two type 070188 boards have been added to the upper card file in positions 22 and 23. These Output Driver boards contain the necessary logic to accept the required Data, Ident, and Control lines. The function of the Output Driver board is to Invert the incoming signals and provide low current logic level drive capability (i.e., Logic 1 = +.4V ±.4V and Logic 0 = +4V ±1V @ 35 MA).

Outputs from the 070188 board are presented to rear panel connectors J3 and J4. Connector J4 contains all the signals present on J3, plus a Main Frame pulse. Although these signals are identical, they are independently buffered from each other. Table 1 identifies the connector contents.

TABLE 1

J3	J4
Data Bit $\overline{1}$	Data Bit $\overline{1}$
Data Bit $\overline{2}$	Data Bit $\overline{2}$
Data Bit $\overline{3}$	Data Bit $\overline{3}$
Data Bit $\overline{4}$	Data Bit $\overline{4}$
Data Bit $\overline{5}$	Data Bit $\overline{5}$
Data Bit $\overline{6}$	Data Bit $\overline{6}$
Data Bit $\overline{7}$	Data Bit $\overline{7}$
Data Bit $\overline{8}$	Data Bit $\overline{8}$
Word ID $\overline{1}$	Word ID $\overline{1}$
Word ID $\overline{2}$	Word ID $\overline{2}$
Word ID $\overline{4}$	Word ID $\overline{4}$
Word ID $\overline{8}$	Word ID $\overline{8}$
Word ID $\overline{10}$	Word ID $\overline{10}$
Word ID $\overline{20}$	Word ID $\overline{20}$
Word ID $\overline{40}$	Word ID $\overline{40}$
$\overline{\text{SEARCH}}$	$\overline{\text{SEARCH}}$
$\overline{\text{VERIFY}}$	$\overline{\text{VERIFY}}$
$\overline{\text{CHECK}}$	$\overline{\text{CHECK}}$
$\overline{\text{LOCK}}$	$\overline{\text{LOCK}}$
	$\overline{\text{MAIN FRAME}}$ *

* Internal signal designated as Main Frame Rate (MF)

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DRAWING LIST CHANGES

Final Assembly changes from 074267 to 074312

Unit Assembly PCM System changes from 074082 to 074311

Wire List 074313 added

Board Assembly 070188	Output Driver Board Added
Logic Diagram 075188	Output Driver Board Added

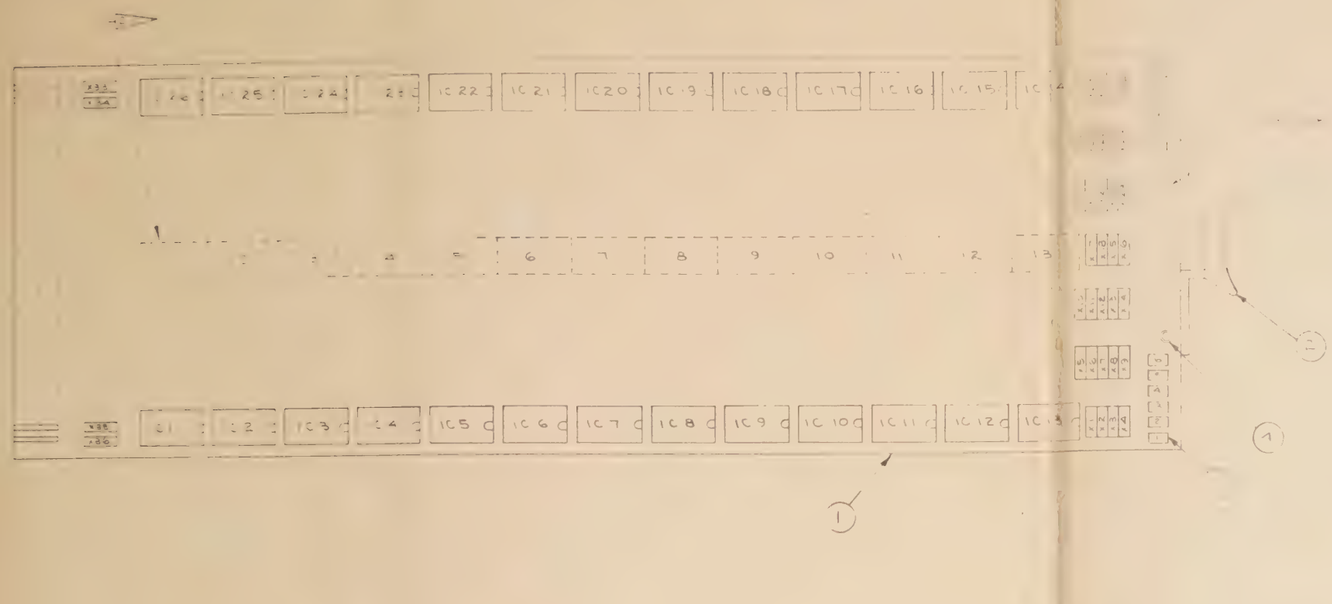
UNIT 4001-000-006 INTERFILE

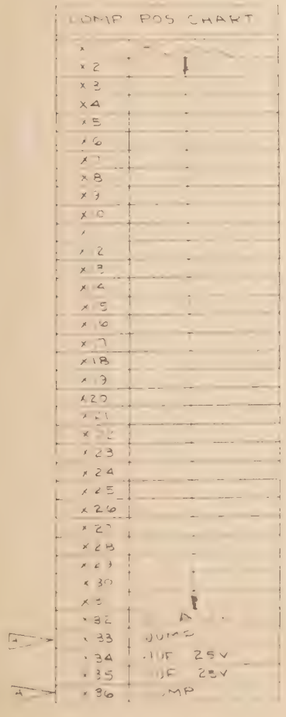
FROM	TO	FROM	TO	FROM	TO
10FL3	22BR2	23GR1	23AL4		
	23BR2	16GL2	22AL5		
10AR5	22BL5		23AL5		
	23BL5	16ER2	22FL5		
10BR4	22BR5		23FL5		
	23BR5	22GR3	22BL2		
10CR1	22CL1	23GR3	23BL2		
	23CL1	16GR2	22FL3		
10DR2	22CR4	22FL2	22FR3		
	23CR4				
10CL5	22CL5				
	23CL5				
10CR4	22DR2				
	23DR2				
10EL1	22CR5				
	23CR5				
10DL4	22AR5				
	23AR5				
18CR2	22DR3				
	23DR3				
18CL2	22DL5				
	23DL5				
18CL3	22ER1				
	23ER1				
18CR3	22EL4				
	23EL4				
18BR5	22ER5				
	23ER5				
18DL1	22EL5				
	23EL5				
18FR5	22GL3				
	23GL3				
16AL3	22AL3				
	23AL3				
16DR4	22GL1				
	23GL1				
22GR1	22AL4				

UNIT 4001-000-006

UPPER FILE TO UPPER REAR PANEL

FROM	TO	FROM	TO	FROM	TO
J4-1	22AR2	J3-1	23AR2		
J4-2	22AR4	J3-2	23AR4		
J4-3	22AR3	J3-3	23AR3		
J4-4	22AL2	J3-4	23AL2		
J4-5	22BR1	J3-5	23BR1		
J4-6	22BR4	J3-6	23BR4		
J4-7	22BL4	J3-7	23BL4		
J4-8	22BR3	J3-8	23BR3		
J4-9	22DR1 22AR1	J3-9	23DR1 23AR1		
J4-10	22DR4	J3-10	23DR4		
J4-11	22DR5	J3-11	23DR5		
J4-12	22ER4	J3-12	23ER4		
J4-13	22EL3	J3-13	23EL3		
J4-14	22ER3	J3-14	23ER3		
J4-15	22EL2	J3-15	23EL2		
J4-16	22ER2	J3-16	23ER2		
J4-17	22CL2	J3-17	23CL2		
J4-18	22CR2	J3-18	23CR2		
J4-19	22CL3	J3-19	23CL3		
J4-20	22CR3	J3-20	23CR3		
J4-22	GND	J3-21	GND		
J4-21	22FR2 22GL4	J3-22	10GL4		
J4-23	8GL4	J3-23	11AR1		
J4-24	9AR1	J3-24	11GL4		
J4-25	9GL4	J3-25	12AR1		





NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE "070-5E REV
2. REPAIR PER SECTION 3-13
3. STAMP ASSEMBLY NO. IN 3/32 HIGH CHARACTERS APPROX AS SHOWN USING WHITE INDELIBLE INK.
4. USE "22 AWG SOLID W. RE.
5. FOR LOGIC SEE 075-182
6. SEE IC POSITION CHART.
7. SEE COMP POSITION CHART.
8. INSTALL TEM-6 IN A HOLES.

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
1	079009		BOARD SUB ASS'Y			
1	AE 6200		CARD PULL	STANFORD APPLIED		2
12	8046-1		TEST JACK	AUGAT		3
2	200-5-02		RIVET			4
2	30023		CAPACITOR .1UF 25V			5
A/R	016467		CONNECTION PIN			6
1	30 GA WIRE		IC			

LIST OF MATERIALS

REF	DESCRIPTION	QTY
A	3/4 DIA #79 DR	A/R

DIMENSIONS AND TOLERANCES PER MIL-STANDARD UNLESS OTHERWISE SPECIFIED. TOLERANCES IN: XXX ±.005 XX ±.01 X ±.1. FRACTIONS ±1/64. ANGLES ±1°. MATERIAL — ± — N — APPROVED — DATE —. NEXT ASSY — USED ON — APPLICATION

CONTRACT NO — DRAWN — DATE — CHECKED — DESIGNER — PROJECT ENG — APPROVED — DATE —

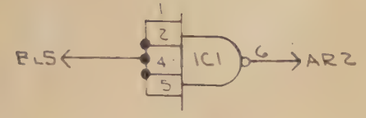
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

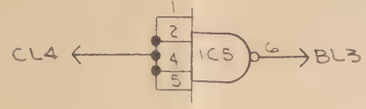
BOARD ASS'Y
OUTPUT DRIVER

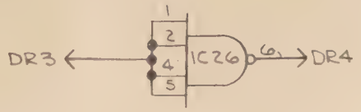
SIZE D | CODE IDENT 08539 | 079189

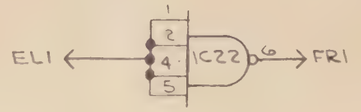
REVISIONS
ZONE | NO | DESCRIPTION | DATE | APPROVED

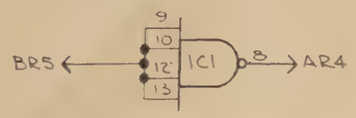
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

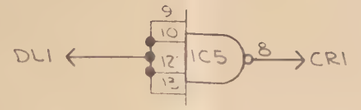


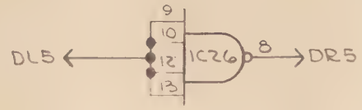


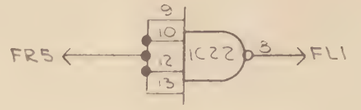


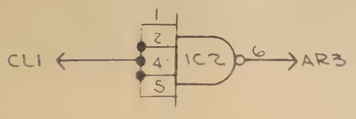


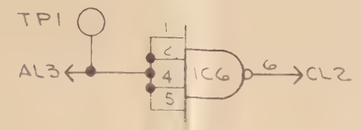


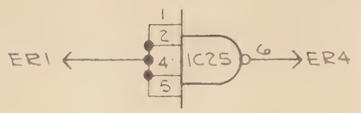


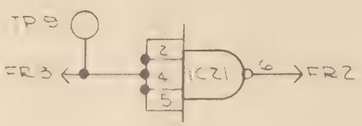


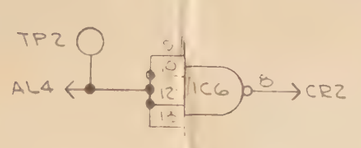


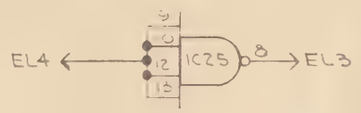


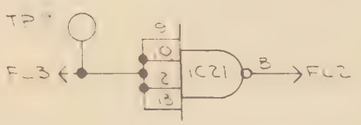


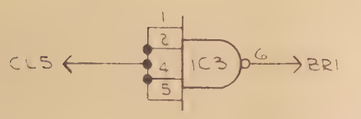


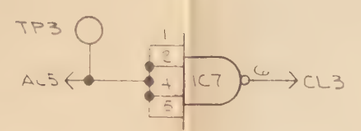


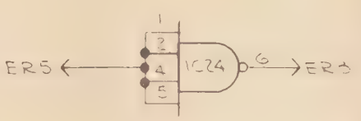


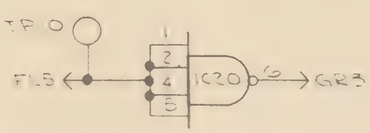


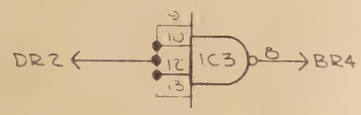


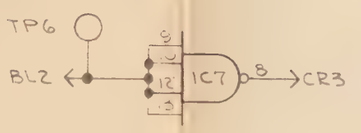


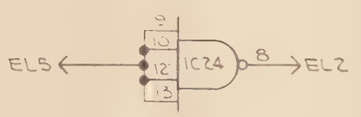


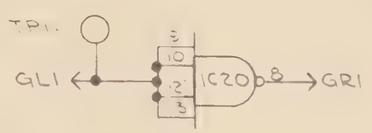


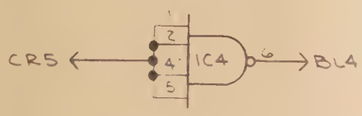


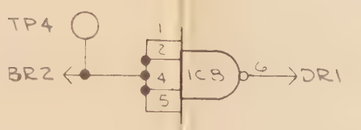


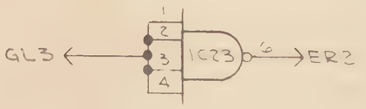


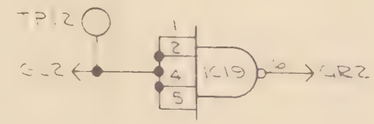


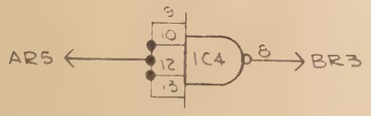


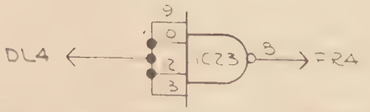












NOTES:
1-ALL IC'S ARE SN7440N.

REF	DESCRIPTION	QTY.

PART OR IDENTIFYING NO.	DESCRIPTION

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
XXX ± XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.		
DRAWN	J.C.LETIZIA	DATE 5/9/69
CHECKED		
DESIGNER		
PROJECT ENG		
APPROVED		
MATERIAL		
FINISH		

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

OUTPUT DRIVER BOARD

SIZE	DWG. NO.	REV
C	08539	075188

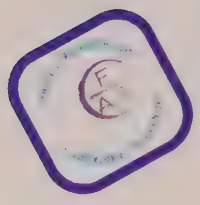
SCALE ± WEIGHT ± SHEET ±

DRAWING NO. DATA-CONTROL SYSTEMS CORPORATION Danbury, Connecticut U.S.A. REPRODUCTION NO. 440V

075188

4 3 2 1

D C B A



INSTRUCTION MANUAL

PCM SYSTEM

MODEL 4001

INSTRUCTION MANUAL

PCM SYSTEM

MODEL 4001

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SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

This instruction manual provides operating and maintenance instructions for the PCM System Model 4001, designed and manufactured by Data Control Systems, Inc., East Liberty Street, Danbury, Connecticut. A general description of the system is given in Section I. Installation (II) and Operation (III) are presented in a manner useful to personnel not familiar with the initial setup and operation of PCM Systems. Since there are few industry standards regarding the definition of PCM terms, a glossary of terms and definitions of PCM terms as used in this manual is given in Section VI.

1.2 INTRODUCTION

The Model 4001 PCM System illustrated in Figure 1-1 is a self-contained universal PCM System which decommutates noisy serial pulse trains and presents, at the system output, parallel data, word identification and strobe. The PCM System consists of three major subsystems; a bit synchronizer, format synchronizer and a select and monitor subsystem, integrated into a complete PCM processing station.

Figure 1-1. Model 4001 PCM Decommutation System

Bit synchronization, in the 4001 PCM System, is accomplished by a Model SBS-2 Bit Synchronizer. This subsystem is a self-contained plug-in module capable of bit synchronization with applied bit rates of from 10 BPS to 1.6 MBS NRZ (5 BPS to 0.8MBS, RZ and Bi-Ø) codes. The bit synchronizer (and 4001 PCM System) accepts RZ, NRZ-L, -M, -S, Bi-Ø-L, -M, -S codes as described in IRIG Document 106-66. Bit rate ranges are changed by a removable internal card. Input signals may be normal or inverted and two loop filters (wide and narrow) are provided for quick synchronization to questionable data.

All format information is contained on a FORMAT STORAGE CARD and read into the system by a front panel card reader. The card is of durable plastic and may be manually punched.

The system utilizes four operating modes to attain and present an indication of format synchronization status: SEARCH, VERIFY, LOCK and CHECK. In the SEARCH mode the system continuously monitors the data for a synchronization pattern. When it arrives, and is recognized; the system is placed in the VERIFY operating mode.

The VERIFY mode is used to increase the confidence that the system is in proper synchronization prior to declaring it so. Front panel controls allow the operator to require from 0 to 15 successive

correct patterns prior to placing the system in LOCK. During this accumulation of correct sync patterns the occurrence of one incorrect pattern will revert the system immediately to the SEARCH mode. While the system is operating in the VERIFY mode (or LOCK and CHECK), the data is monitored for a synchronization pattern only during the time at which it is expected to appear, so that a correct pattern is a synchronization pattern which appears at the expected time and is recognized as a sync pattern. Conversely, an incorrect pattern is one which either does not arrive at the expected time or is not recognized as a synchronization pattern (due to bit errors). The expected time is predicted on the basis of the format information (words/frame, bits/word, etc.) and the detection of the first synchronization pattern while the system is in the SEARCH mode.

Upon the accumulation of the required number of correct patterns, the system is transferred from VERIFY to the LOCK mode. The LOCK mode constitutes a declaration by the system that proper synchronization is being maintained. The system remains in this mode until one incorrect synchronization pattern transfers it to CHECK.

When in the CHECK mode the operator may require the accumulation of from 0 to 15 incorrect patterns prior to transferring the system to SEARCH. If during this accumulation one correct synchronization pattern is detected the system is reverted to LOCK.

Any word of the PCM data being processed may be selected for front panel display by the select and monitor subsystem. Words are displayed digitally and simultaneously, its analog equivalent is indicated on a front panel mounted meter. Application of the selected word to peripheral equipment is readily accomplished since a voltage proportional to the analog value is available at a rear panel connector.

The 4001 PCM System is designed for installation in standard 19-inch instrumentation racks and is a self-contained unit in that it is self cooling and requires only commercial power for operation.

Access to the internal circuitry of the system is achieved through the front and rear panel, both of which are mounted on hinges which allow them to swing open without impeding the system operation.

1.3 AVAILABLE MODELS

There are four standard models of the 4001 PCM System. Each model and their capabilities are described below.

1.3.1 Model 4001-000

This model is the basic building block upon which all subsequent models are constructed. This model is capable of main frame synchronization and correlation with main frame synchronization patterns of up to 33 bits in length.

1.3.2 Model 4001-100

This model contains all the capabilities of the -000 plus the ability to process data containing Frame Code Complement (FCC) or Frame Alternating Complement synchronization patterns. A PCM format utilizing a Frame Code Complement (FCC) synchronization pattern is one in which the synchronization pattern data value is complemented once per subframe in order to identify the cycle of the subframe. With this method a number of subframes may be synchronized by the PCM System if they are synchronous and the length of each is a sub-multiple of the longest subframe cycle rate.

A Frame Alternating Complement (FAC) synchronization pattern is not generally used for subframe synchronization, but is adopted to provide additional confidence in the main frame synchronization. An FAC synchronization pattern is one in which the sync pattern is complemented every other frame, and is effective in preventing the system from LOCKing on repetitive data similar to the synchronization pattern.

In addition to the main frame operating modes of SEARCH, VERIFY, LOCK and CHECK, a capability which all models of the 4001 PCM System possess, the -100 provides subframe operating modes of SEARCH, LOCK and CHECK. These modes perform similarly as the main frame operating modes except that the main frame operating status maintains a priority over all subframe modes. If the main frame mode transfers to SEARCH, the subframe mode returns to SEARCH also.

1.3.3 Model 4001-110

In addition to all the capabilities of the -100 model, this model is capable of subframe synchronization to Unique Recycling Codes (URC). A Unique Recycling Code is a subframe synchronization pattern which is usually located in a different word position than the main frame synchronization pattern and which appears once per subframe. More than one subframe may be synchronized by this method as long as they are synchronous and the length of each is a sub-multiple of the longest subframe.

In addition to the main frame operating modes of SEARCH, VERIFY, LOCK and CHECK, a capability which all models of the 4001 PCM System possess, the -110 provides subframe operating modes of SEARCH, VERIFY, LOCK and CHECK. These modes perform similarly to the main frame operating modes, except that the main frame operating status maintain a priority over all subframe modes. If the main frame mode transfers to SEARCH, the subframe mode returns to SEARCH also.

1.3.4 Model 4001-111

This model offers the capability, in addition to those of the -110 model, of processing data containing subframe identification synchronization patterns (SFID). A PCM format which contains SFID, utilizes several consecutive bits located anywhere in the frame to provide identification to subframe words. The SFID bits change at the frame rate usually in some binary counting method. The SFID is generally adopted to place a unique count within each transmitted frame for identification. In this manner subframe identification begins immediately, without waiting for a specific pattern appearing at the subframe rate.

Subframe operating modes are SEARCH, VERIFY, LOCK and CHECK which operate as in the -110 model with the main frame operating mode exercising priority.

1.4 PHYSICAL CHARACTERISITCS

The Model 4001 PCM System, illustrated in Figure 1-1, is contained in an aluminum chassis and cover finished in plated chromate. Standard front panels are gray with black lettering. Other salient physical specifications are:

Dimensions:	10.5" high, 20" deep - mounts in a standard 19" instrumentation rack
Weight:	52 pounds
Power:	115 VAC, 60 Hz
Recommended Slides:	Configuration does not require slides for internal accessability. However, if slides are preferred the recommendation is Jonathan Mfg. Corp. 110QD-20-2

1.5 ELECTRICAL CHARACTERISTICS

1.5.1 Bit Synchronization

Input Impedance:	10,000 ohms
Input Levels:	0.5 to 25 volts peak-to-peak without adjustment.
Input Dynamic Range:	34db
Input Code Formats:	RZ, NRZ-L, -M, -S, Bi-Phase-L, -M, -S as defined in IRIG Document 106-66, Punch Card Programmable.
Bit Rate:	10 BPS to 1.6 MBPS - NRZ, 5 BPS to 800 KBPS - RZ & Bi-Phase.
Selector Bit Rate Range:	Each bit rate selector card, SBS-2/TU covers a range of 1.6:1 (see Table 1-1)
Input Polarity:	Normal or inverted, selectable by front panel switch.
Synchronization Maintainability:	Unit maintains bit synchronization when signal to noise degrades to -6db. (Measured with NRZ signal with maximum transition density filtered by a 36db/octave Gaussian filter. Cutoff at 0.5 bit rate with superimposed Gaussian noise bandlimited to 0.5 bit rate.

Table 1-1. SBS-2/TU Bit Rate Selector Plug-in Cards

Type Number	Bit Rate Range (NRZ)	Bit Rate Range RZ and Bi-Phase)
1	10 - 16 BPS	5 - 8 BPS
2	16 - 25 BPS	8 - 12 BPS
3	25 - 40 BPS	12.5 - 20 BPS
4	40 - 65 BPS	20 - 32.5 BPS
5	65 - 100 BPS	32.5 - 50 BPS
6	100 - 160 BPS	50 - 80 BPS
7	160 - 250 BPS	80 - 125 BPS
8	250 - 400 BPS	125 - 200 BPS
9	400 - 650 BPS	200 - 325 BPS
10	650 - 1000 BPS	325 - 500 BPS
11	1 - 1.6 KBS	500 - 800 BPS
12	1.6 - 2.5 KBS	800 - 1250 BPS
13	2.5 - 4 KBS	1.25 - 2 KBS
14	4 - 6.5 KBS	2 - 3.25 KBS
15	6.5 - 10 KBS	3.25 - 5 KBS
16	10 - 16 KBS	5 - 8 KBS
17	16 - 25 KBS	8 - 12.5 KBS
18	25 - 40 KBS	12.5 - 20 KBS
19	40 - 65 KBS	20 - 32.5 KBS
20	65 - 100 KBS	32.5 - 50 KBS
21	100 - 160 KBS	50 - 80 KBS
22	160 - 250 KBS	80 - 125 KBS
23	250 - 400 KBS	125 - 200 KBS
24	400 - 650 KBS	200 - 325 KBS
25	650 - 1000 KBS	325 - 500 KBS
26	1000 - 1600 KBS	500 - 800 KBS

Transition Density:	Unit will maintain synchronization with repetitive patterns of one bit status change in 128 bit periods (NRZ data)
Tracking Rate:	With a 0.2% bit rate variation frequency:

Bit Rate:	p-p width/bit variation
10 BPS to 100 BPS NRZ (wide loop):	60%
10 BPS to 100 BPS NRZ (narrow loop):	10%
100 BPS to 1.6 MBPS (wide loop):	10%
100 BPS to 1.6 MBPS (narrow loop):	1%

Loop Stability:	±0.8% of preset bit rate
Base Line Shift:	Unit maintains synchronization when the data base line is shifted by a superimposed triangular waveform with an amplitude of 400% of the data and a frequency 0.1% of the data bit rate. Maximum shift is ±12.5 volts.

1.5.2 Format Synchronization (all models)

Bits per Word:	2-12 punch card programmable (syllabilized words to 64 bits, 16 syllables per word, 2 syllable lengths per word)
Words per Frame:	Up to 4,096
Frame Sync Pattern:	Up to 33 bits
Parallel Data Outputs:	Up to 12 bits
Synchronization Modes:	4, SEARCH, VERIFY, LOCK CHECK
Synchronization Aperture	1, 3, or 5 bits programmable

1.5.3 Format Synchronization 4001-100

Words per frame:	Up to 4,096
Frames per Subframe:	Up to 4,096
Frame Synchronization Pattern:	Up to 33 bits programmable
Frame Code Complement Pattern:	The Complement of the frame sync pattern in the same location at the subframe cycle rate
Frame Alternating Complement Pattern:	The complement of the frame sync pattern in the same frame location in alternate frames
Synchronization Modes:	Frame - SEARCH, VERIFY, LOCK, CHECK Sub-frame - SEARCH, LOCK, CHECK

1.5.4 Format Synchronization 4001-110

Words per frame:	Up to 4,096
Frames per Subframe:	Up to 4,096
Frame Synchronization Pattern:	Up to 33 bits programmable
Subframe Synchronization Pattern:	Up to 33 bits any location in frame
Synchronization Modes:	Frame - SEARCH, VERIFY, LOCK, CHECK Subframe - SEARCH, VERIFY, LOCK, CHECK

1.5.5 Format Synchronization 4001-111

Words per Frame:	Up to 4,096
Frames per Subframe:	Up to 256
Frame Synchronization Pattern:	Up to 33 bits programmable
SFID Word Length:	Up to 8 consecutive bits in any frame word
SFID Location:	Any position in a word, any word within a frame
SFID Start Value:	Binary or BCD "0" or "1" programmable
Synchronization Modes:	Frame - SEARCH, VERIFY, LOCK, CHECK Subframe - SEARCH, VERIFY, LOCK, CHECK

SECTION II

INSTALLATION

2.1 GENERAL

This section describes the procedures necessary for the installation of the Model 4001 PCM System.

The scope of this section encompasses the initial installation, connection of power and Data Lines but precludes actual operation of the equipment.

2.2 UNPACKING AND HANDLING

The Model 4001 PCM System and all necessary equipment is shipped, sealed in a moisture proof polyethelene bag and wrapped in Kimpack insulating material to absorb shock during transportation. Remove the unit from its container and perform a general visual inspection. Retain all packing and shipping materials until this inspection is completed.

If the visual inspection discloses physical damage or if during subsequent testing, the System does not meet operating specifications immediately notify the carrier and the nearest DCS Field Office or

Field Service Department
Data-Control Systems, Inc.
East Liberty Street
Danbury, Connecticut 06810

2.3 MOUNTING

The PCM System is designed for mounting on angles, and with complete access to the unit attainable thru the front or rear, there is no need for slide mounting. However, the System may also be mounted on drawer type slides (Jonathan Mfg. Corp. or equivalent) if preferred. Two tapped holes are provided (8-32) for the mounting of slides and are located in drawing 074042 which may be found at the rear of this instruction manual.

After fastening the angles or slides (not supplied) mount the System in the assigned rack position and connect all necessary cables.

2.4 INTERCONNECTION

The System is shipped with all mating connectors necessary to complete the integration of the Decommutation System into a PCM Ground Station. Table 2-1 contains a list of all rear panel connectors and pins, the function of each, and the wire size recommended for proper system operation.

2.5 COOLING

The PCM Decommutation System is equipped with a muffin fan which delivers adequate quantities of cooling air for proper oper-

ation. The System therefore may be operated without additional rack cooling if it is assured that ambient environmental stresses do not exceed those specified.

Table 2-1. Rear Panel Connectors and Pins

Connector/ Pin	Function	Recommended Wire Gauge
J1-1	115 VAC	#12 AWG } Input
J1-2	115 VAC	#12 AWG } Requirement
J1-3	Ground	#12 AWG }
J2-1	+24 VDC Output . 5 ampere	#18 AWG } These voltages
J2-2	+24 VDC Return . 5 ampere	#18 AWG } are not input re-
J2-3	-24 VDC Output . 5 ampere	#18 AWG } quirements but
J2-4	-24 VDC Return . 5 ampere	#18 AWG } are available for
J2-5	+5 VDC Output 11 ampere	#18 AWG } use in other areas
J2-6	+5 VDC Return 11 ampere	#18 AWG } such as a DCS
J2-7	+5 VDC Output 11 ampere	#18 AWG } Model 4221 Word
J2-8	+5 VDC Return 11 ampere	#18 AWG } Selector.
J3-1	Word Counter Section 1 $\overline{1}$	#24 AWG
J3-2	Word Counter Section 1 $\overline{2}$	#24 AWG
J3-3	Word Counter Section 1 $\overline{4}$	#24 AWG
J3-4	Word Counter Section 1 $\overline{8}$	#24 AWG
J3-5	Word Counter Section 2 $\overline{1}$	#24 AWG
J3-6	Word Counter Section 2 $\overline{2}$	#24 AWG
J3-7	Word Counter Section 2 $\overline{4}$	#24 AWG
J3-8	Word Counter Section 2 $\overline{8}$	#24 AWG
J3-9	Word Counter Section 3 $\overline{1}$	#24 AWG
J3-10	Word Counter Section 3 $\overline{2}$	#24 AWG
J3-11	Word Counter Section 3 $\overline{4}$	#24 AWG
J3-12	Word Counter Section 3 $\overline{8}$	#24 AWG
J3-13	Frame Counter Section 1 $\overline{1}$	#24 AWG
J3-14	Frame Counter Section 1 $\overline{2}$	#24 AWG
J3-15	Frame Counter Section 1 $\overline{4}$	#24 AWG
J3-16	Frame Counter Section 1 $\overline{8}$	#24 AWG
J3-17	Frame Counter Section 2 $\overline{1}$	#24 AWG
J3-18	Frame Counter Section 2 $\overline{2}$	#24 AWG
J3-19	Frame Counter Section 2 $\overline{4}$	#24 AWG
J3-20	Frame Counter Section 2 $\overline{8}$	#24 AWG
J3-21	Frame Counter Section 3 $\overline{1}$	#24 AWG
J3-22	Frame Counter Section 3 $\overline{2}$	#24 AWG
J3-23	Frame Counter Section 3 $\overline{4}$	#24 AWG
J3-24	Frame Counter Section 3 $\overline{8}$	#24 AWG

Table 2-1. Rear Panel Connectors and Pins (continued)

Connector/ Pin	Function	Recommended Wire Gauge
J3-25	Digital Data Output 1 (most significant bit)	#24 AWG
J3-26	Digital Data Output 2	#24 AWG
J3-27	Digital Data Output 3	#24 AWG
J3-28	Digital Data Output 4	#24 AWG
J3-29	Digital Data Output 5	#24 AWG
J3-30	Digital Data Output 6	#24 AWG
J3-31	Digital Data Output 7	#24 AWG
J3-32	Digital Data Output 8	#24 AWG
J3-33	Digital Data Output 9	#24 AWG
J3-34	Digital Data Output 10	#24 AWG
J3-35	Digital Data Output 11	#24 AWG
J3-36	Digital Data Output 12 (least significant bit)	#24 AWG
J3-37	Data Strobe	#24 AWG
J3-38	Frame Rate	#24 AWG
J3-39	Sub-Frame Rate	#24 AWG
J4-1	Identification Word Counter Section 1 1	#24 AWG
J4-2	Identification Word Counter Section 1 2	#24 AWG
J4-3	Identification Word Counter Section 1 4	#24 AWG
J4-4	Identification Word Counter Section 1 8	#24 AWG
J4-5	Identification Word Counter Section 2 1	#24 AWG
J4-6	Identification Word Counter Section 2 2	#24 AWG
J4-7	Identification Word Counter Section 2 4	#24 AWG
J4-8	Identification Word Counter Section 2 8	#24 AWG
J4-9	Identification Word Counter Section 3 1	#24 AWG
J4-10	Identification Word Counter Section 3 2	#24 AWG
J4-11	Identification Word Counter Section 3 4	#24 AWG
J4-12	Identification Word Counter Section 3 8	#24 AWG
J4-13	Identification Frame Counter Section 1 1	#24 AWG
J4-14	Identification Frame Counter Section 1 2	#24 AWG
J4-15	Identification Frame Counter Section 1 4	#24 AWG
J4-16	Identification Frame Counter Section 1 8	#24 AWG
J4-17	Identification Frame Counter Section 2 1	#24 AWG
J4-18	Identification Frame Counter Section 2 2	#24 AWG
J4-19	Identification Frame Counter Section 2 4	#24 AWG
J4-20	Identification Frame Counter Section 2 8	#24 AWG
J4-21	Identification Frame Counter Section 3 1	#24 AWG
J4-22	Identification Frame Counter Section 3 2	#24 AWG
J4-23	Identification Frame Counter Section 3 4	#24 AWG
J4-24	Identification Frame Counter Section 3 8	#24 AWG
J4-25	Digital Data Output 1 (most significant bit)	#24 AWG
J4-26	Digital Data Output 2	

Table 2-1. Rear Panel Connectors and Pins (continued)

Connector/ Pin	Function	Recommended Wire Gauge
J4-27	Digital Data Output 3	#24 AWG
J4-28	Digital Data Output 4	#24 AWG
J4-29	Digital Data Output 5	#24 AWG
J4-30	Digital Data Output 6	#24 AWG
J4-31	Digital Data Output 7	#24 AWG
J4-32	Digital Data Output 8	#24 AWG
J4-33	Digital Data Output 9	#24 AWG
J4-34	Digital Data Output 10	#24 AWG
J4-35	Digital Data Output 11	#24 AWG
J4-36	Digital Data Output 12 (least significant bit)	#24 AWG
J4-37	Data Strobe	#24 AWG
J4-38	Frame Rate	#24 AWG
J4-39	Sub-Frame Rate	#24 AWG
J4-40	No Connection	#24 AWG
J4-41	$\overline{\text{Advance}}$	#24 AWG
J4-42	Last Count Frame	#24 AWG
J4-43	Last Count Sub-Frame	#24 AWG
J4-44	Search #1	#24 AWG
J4-45	Lock #1	#24 AWG
J4-46	Search #2	#24 AWG
J4-47	Lock #2	#24 AWG
J5	Data Input	RG174/U
J6	No Connection	RG174/U
J7	Serial NRZ Output	RG174/U
J8	Clock Output	RG174/U
J9	Analog Data Output	RG174/U

SECTION III

OPERATION

3.1 GENERAL

This section contains a description of the controls and indicators (figure 3-1) initial adjustments, operating procedures, and programming instructions associated with the 4001 PCM Decommutation System.

3.2 CONTROLS AND INDICATORS

The controls and indicators, their function and location are listed in Table 3-1 below:

Table 3-1. Controls and Indicators

Control/Indicator	Location	Function
NORM/INV Switch	BIT SYNC (upper left)	Standardizes the input to Bit Synchronizer with normal or inverted data applied
WIDE/NAR	BIT SYNC (upper left)	Selects loop filter bandwidth in the synchronizer
OPER/SET	BIT SYNC (upper left)	Opens (SET) and closes(OPER) phase lock loop on synchronizer causing the input to the meter circuit to be either the band center frequency of the internal VCO (SET) or the frequency difference between data and VCO (OPER)

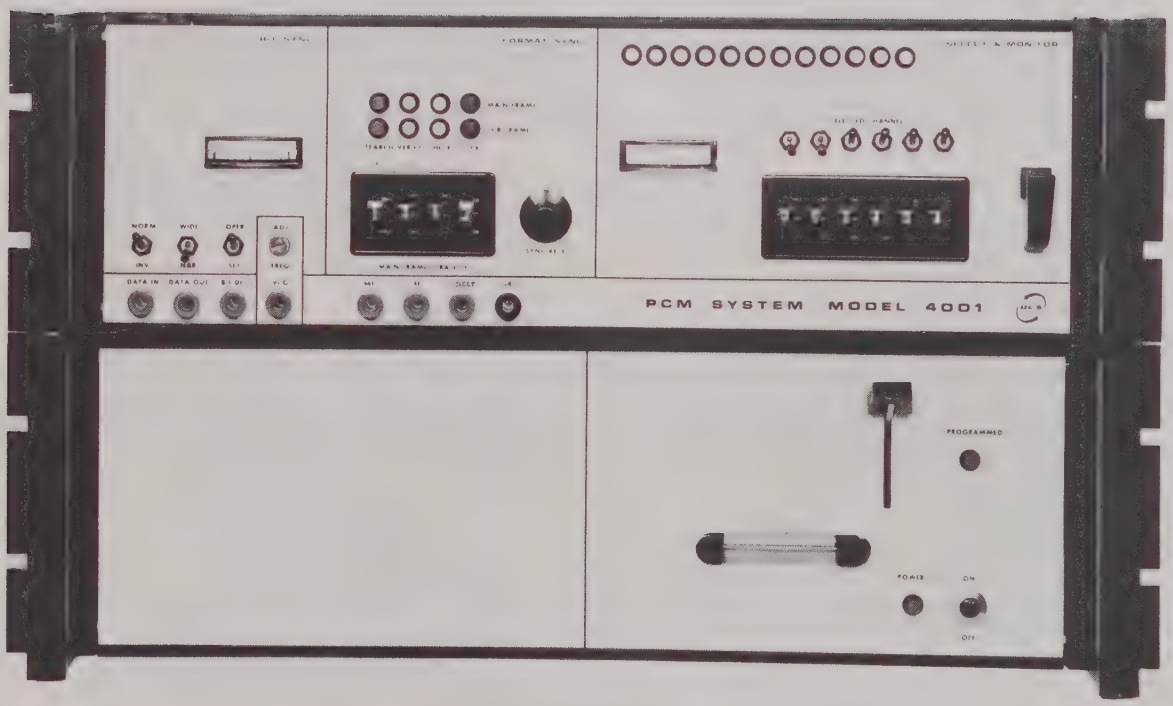


Figure 3-1. Front Panel, 4001 PCM Decommutation System

Table 3-1. Controls and Indicators (continued)

Control/Indicator	Location	Function
Meter	BIT SYNC (upper left)	Indicates probability of error when OPER/SET switch is in OPER. When in SET meter indicates frequency difference between internal VCO and the input Data.
DATA IN	BIT SYNC (upper left)	Monitor point for the input data to the bit synchronizer
DATA OUT	BIT SYNC (upper left)	Monitor point for the output of the bit synchronizer
BIT DET	BIT SYNC (upper left)	Monitor point for the bit detector output
ADJ FREQ	BIT SYNC (upper left)	Adjusts frequency of the bit synchronizer's voltage controlled oscillator
VCO	BIT SYNC (upper left)	Monitor point for the voltage controlled oscillator output
MAIN FRAME/ SEARCH (Red) indicator	Format Sync (upper center)	Indicates main frame synchronization status in SEARCH
MAIN FRAME/ VERIFY (orange) indicator	Format Sync (upper center)	Indicates the main frame synchronization status in VERIFY
MAIN FRAME/ CHECK (yellow) indicator	Format Sync (upper center)	Indicates the main frame sync status in CHECK
MAIN FRAME/ LOCK (green) indicator	Format Sync (upper center)	Indicates the main frame sync status in LOCK

Table 3-1. Controls and Indicators (continued)

Control/Indicator	Location	Function
SUB-FRAME/ SEARCH (red)	Format Sync (upper center)	Indicates sub-frame sync status in SEARCH
SUB-FRAME/ VERIFY (orange) indicator	Format Sync (upper center)	Indicates sub-frame sync status in VERIFY
SUB-FRAME/ CHECK (yellow) indicator	Format Sync (upper center)	Indicates sub-frame sync status in CHECK
SUB-FRAME/ LOCK (green) indicator	Format Sync (upper center)	Indicates sub-frame sync status in LOCK
MAIN FRAME STRATEGY Thumb-wheel Switches:		
ℓ_s	Format Sync (upper center)	SEARCH mode bit error tolerance control. Thumbwheel allows from 0 to 9 errors in the Main Frame Sync Pattern while in the SEARCH mode
Σ_v	Format Sync (upper center)	VERIFY accumulator control thumbwheel. Allows accumulation of from 0 to 15 consecutive correct main frame sync patterns before advancing to LOCK
Σ_c	Format Sync (upper center)	CHECK accumulator control thumbwheel. Allows accumulation of from 0 to 15 consecutive incorrect main frame sync patterns before returning to SEARCH
$\ell_{\overline{S}}$	Format Sync (upper center)	$\overline{\text{SEARCH}}$ mode bit error tolerance control. Thumbwheel allows from 0 to 9 bit errors in the main frame sync pattern while in VERIFY, LOCK and CHECK modes

Table 3-1. Controls and Indicators (continued)

Control/Indicator	Location	Function
SYNC RESET switch	Format Sync (upper center)	Resets all correlators to SEARCH mode
MF monitor point	Format Sync (upper center)	Gives pulse at frame rate corresponding to first word of frame
SF monitor point	Format Sync (upper center)	Gives pulse at sub-frame rate corresponding to first word of the first sub-frame
SELECT monitor point	Format Sync (upper center	D/A output of selected word
GRD monitor point	Format Sync (upper center)	Signal ground
Display Lamps (12 ea.)	Select and Monitor upper right	Displays selected word binarily
Meter	Select and Monitor (upper right)	Displays selected word analog
SELECTED CHANNEL switches (6 ea.)	Select and Monitor (upper right)	Deactivates corresponding thumbwheel SELECTED CHANNEL switches
Switches (thumbwheel) (6 ea.)	Select and Monitor (upper right)	Allows selection of a specific word for D/A conversion and display

Table 3-1. Controls and Indicators (continued)

Control/Indicator	Location	Function
CARD READER	Lower Right	Card reader is activated by inserting programmed format storage card in card slot. The format storage card may be removed by depressing the card reader handle
PROGRAMMED Indicator	Lower Right	Indicates program card is inserted and locked
POWER Indicator	Lower Right	Indicates 115 VAC applied to the system
ON/OFF Switch	Lower Right	Controls facility power

3.3 OPERATION

Operation of the 4001 Word Selector consists of:

a. Setting up the equipment to accommodate the PCM format being decommutated.

b. Checking out the equipment.

c. Applying the data to be decommutated.

3.3.1 Operating Notes - Bit Synchronizer Section

The WIDE/NAR switch located in the Bit Synchronizer section of the 4001 PCM system is used to optimize the system operation. The position of this switch determines the bandwidth of the loop filter contained in the phase lock loop circuitry of the synchronizer. The narrower the filter bandwidth the greater the noise improvement of the data so that whenever possible the system should be operated with this switch in the NAR position. Unfortunately, however, the narrower the filter bandwidth is, the less allowable data jitter, so that in many applications operation in the WIDE position is mandatory.

If the characteristics of the input data are known, prior to decommutation Figure 3-2 may be used to determine the loop filter bandwidth. If the input characteristics are unknown, it is suggested that the NAR position be initially used and if a continual loss of lock is experienced, as evidenced by the synchronizer meter, revert to the WIDE position. It has been assumed that system noise is at such a level as to warrant a NAR filter position. If relatively clean data is applied to the system with jitter the salient consideration the WIDE/NAR switch should be placed in the WIDE position.

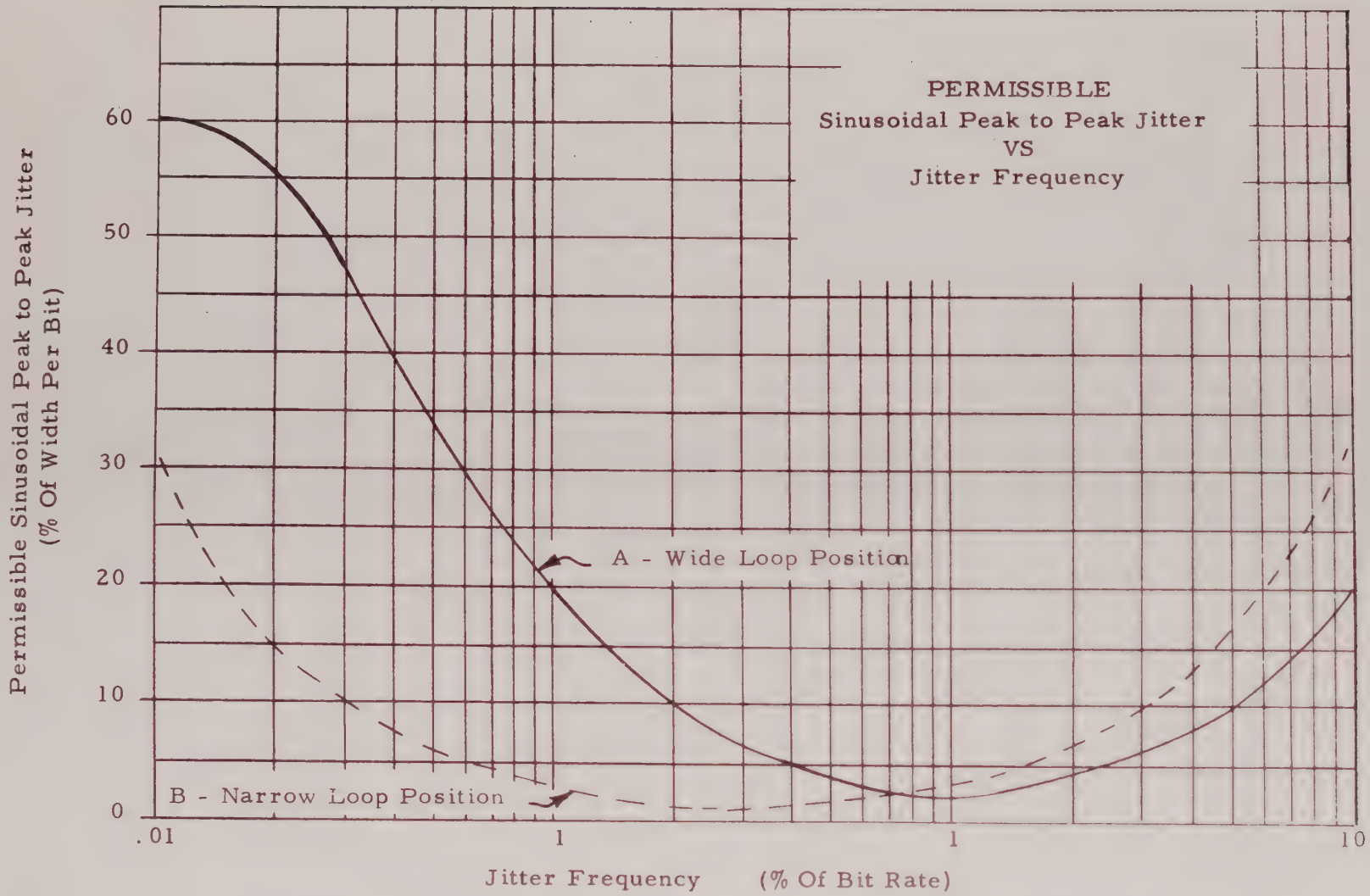


Figure 3-2. Peak-To-Peak Jitter vs Jitter Frequency, 4001 PCM System

The meter located on the front panel of the Bit Synchronizer section provides a measure of bit synchronization quality. With the OPER/SET switch in the OPER position the meter indicates the beat frequency between the data input frequency and the voltage controlled oscillator in the synchronizer, modified some what by the fact that a low pass filter is installed in the meter circuit. As the VCO frequency approaches the input data frequency, the magnitude of the meter reading increases to some maximum as the beat frequency approaches the pass band of the filter. When the beat frequency reaches the filter pass band the meter will behave as a normal beat frequency indicator. That is the oscillating frequency of the meter needle is reduced as the VCO frequency approaches the data frequency and stops when frequencies agree. The magnitude of the indication approaches zero as the phase difference approaches zero.

Since a zero stable reading is obtained with perfect bit synchronization the magnitude of the reading and its stability is a measure of bit synchronization quality.

3.3.2 Operating Notes - Format Synchronizer Section

Synchronization strategy consists of setting the CHECK & VERIFY accumulators and the error tolerance controls located on the front panel of the 4001 PCM System and the FORMAT STORAGE CARD in such a manner that a predetermined degree of confidence in the output data is realized. Some of the more salient factors affecting the selection of a strategy are:

a. The nature of the Analog Data.

b. The quality of the Analog Data.

c. The quality of the PCM Data.

d. The specific areas of interest in a given data reduction run.

For these reasons no step by step procedure is or can be given regarding specific strategy and emphasis is placed on the thorough understanding of the purpose and effect of the strategy controls and the operating sequence.

The error tolerance controls e_s and e_s are used to define the synchronization pattern confidence. From 0 to 9 errors may be selected. The selection of a number of errors in the SEARCH mode (e_s) with the thumbwheels dictates that the selected number of errors may appear in the synchronization pattern and still be recognized by the pattern recognizer circuits as a synchronization pattern. For instance, if

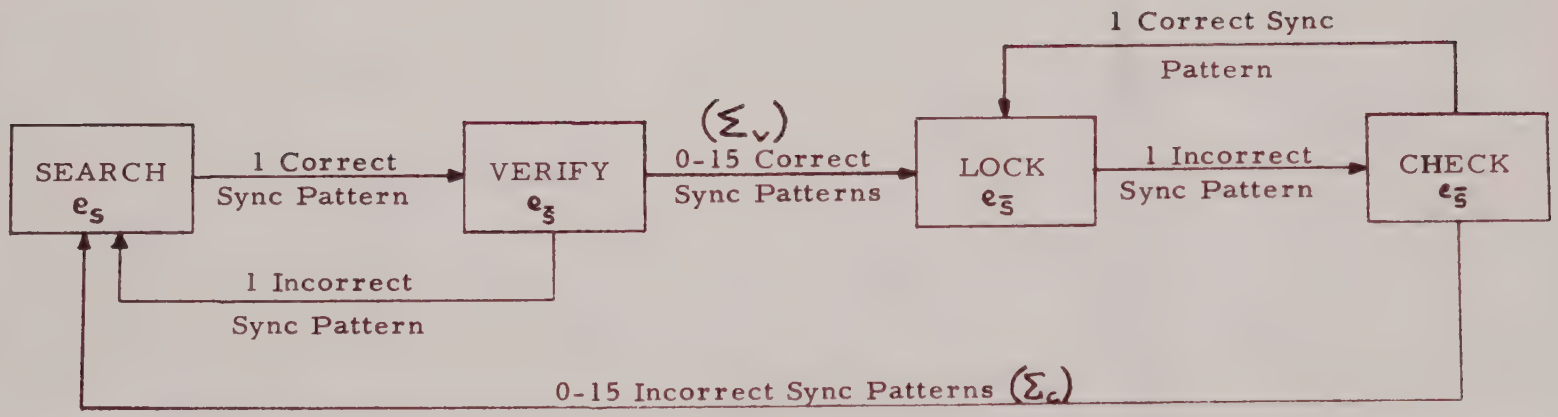
the system is in SEARCH and e_s is set to 9, only 24 bits out of a 33 bit sync pattern need be correct to place the system in the VERIFY mode. However, also remember that 24 data bits looking like a sync pattern with nine errors will also place the system in the VERIFY mode. The $\overline{\text{SEARCH}}$ error tolerance control operates similarly when the system is in a $\overline{\text{SEARCH}}$ mode of operation (i.e. VERIFY, LOCK, CHECK).

Two independent controls are given because the danger of false pattern recognition is not the same in SEARCH and $\overline{\text{SEARCH}}$ modes. While the system is in SEARCH, the correlator circuits are continuously monitoring the pattern recognizer for an indication of sync pattern recognition, and the probability of recognizing a false pattern, that is, some data which looks like a sync pattern is directly related to the setting of the error tolerance control e_s. When the system is in a $\overline{\text{SEARCH}}$ mode, however, the correlator will monitor the pattern recognizer for an indication of sync pattern recognition only during those times at which it is expected to appear. The probability of recognizing a false pattern therefore is greatly reduced, a fact normally influencing a more lenient setting on the error tolerance control while in $\overline{\text{SEARCH}}$.

There are four operating modes to the 4001 PCM System: SEARCH VERIFY, LOCK and CHECK. The nature of each is given below and illustrated in Figure 3-3.

a. SEARCH - While in this mode, the system continuously monitors the data in the shift register for a synchronization pattern; and upon its receipt transfers the system to VERIFY. The Bit, Word, and Frame Counters are reset upon receipt of a sync pattern.

b. VERIFY - In this mode, designed to increase confidence in system synchronization prior to placing it in LOCK, the data is monitored for the sync pattern only during that time at which it is expected (programmed aperture). From 0 to 15 consecutive sync patterns (Σ_v) may be required at the proper time prior to placing the system in LOCK. One sync pattern not appearing at this time will revert the system to SEARCH. When the system is in any operating mode, data from the storage register is not inhibited and evaluation of its validity should take into account the sequence of the operating modes as well as the mode in which it is operating. For instance, if the system is in VERIFY; and it transfers to LOCK it is probably valid. If it reverts to SEARCH it probably is valid.



An incorrect sync pattern is a sync pattern which does not arrive at the expected time or data which is mistaken as a sync pattern

Figure 3-3. Operating Modes of 4001 PCM System

c. LOCK - In this mode the data is monitored for the synchronization pattern only at the aperture time. Correct patterns will maintain the LOCK mode, while one incorrect pattern will place the system in CHECK.

d. CHECK - In this operating mode the system monitors the data for the sync pattern only during aperture time. From 0 - 15 consecutive incorrect sync patterns ($\sum_c$) are required prior to placing the system to SEARCH. Any correct pattern during this accumulation will revert the system to LOCK. The CHECK and VERIFY modes are inversely related. In VERIFY, an accumulation of correct patterns are necessary prior to transferring to LOCK while one incorrect pattern will revert the system to SEARCH. Relatively it is easier to go to SEARCH than LOCK from this mode, a fact which may influence the number of errors selected in a strategy. On the other hand, in CHECK an accumulation of incorrect patterns is necessary prior to transferring to SEARCH while one correct pattern returns the system to LOCK. Therefore, it is easier to transfer to LOCK than SEARCH from this mode, which may also influence the selection of a sync strategy.

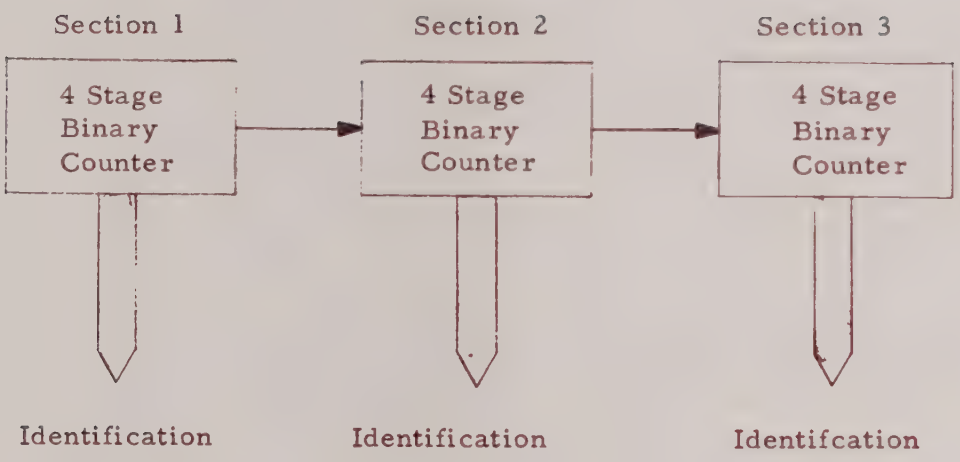
It is important to note that no operating mode alters or impedes the outputting of data in any way. The various modes and mode indicators merely supply a basis for the evaluation of that output data.

3.3.3 Operating Notes - Select and Monitor Section

During the decommutation of data any channel may be selected for digital and analog display in the select and monitor section of the 4001 PCM System. To accomplish this selection, six thumbwheel and six toggle switches are located on the front panel. The operation of these switches is best understood through reference to Figure 3-4.

Word and Frame identification (and hence word selection) is supplied by the word and frame counters respectively located in the format synchronizer section. The identification consists of the binary count contained in the counters at any given time. These counters consist of 3 sections each section of which contains a 4 stage binary counter and which may be reset individually at any count. This and other provisions allow the counters to be configured as a binary coded variable radix counter capable of counting to any base from 2 to 16. The configuration of the counter is discussed in further detail in paragraphs 3.4 and 4.17.

When selecting a word for display, consideration must be given to counter configuration. The six thumbwheel switches (SELECTED CHANNEL) are each associated with a specific section of the word or frame counters and to select a word the specific count in each section must be dialed (decimally).



To select any word the binary count of each section is dialed (decimally) on the SELECTED CHANNEL switches.

Figure 3-4. Word and Frame Counters

From right to left the thumbwheels select:

Word Counter	Section 1
Word Counter	Section 2
Word Counter	Section 3
Frame Counter	Section 1
Frame Counter	Section 2
Frame Counter	Section 3

As an example, consider a word counter configuration which counts to the base 10 (BCD counter). To select the 17th word, the thumbwheel for Section 1 is dialed (6) and the thumbwheel for Section 2-(1) and the thumbwheel for Section 3-(0) since in BCD the count is:

Section 3	Section 2	Section 1
0000	0001	0110

On the other hand if the counter is counting to the base 7; the 17th word is as indicated below

Section 1	thumbwheel - 3	0010
Section 2	thumbwheel - 2	0010
Section 3	thumbwheel - 0	0000

The toggle switches located over each thumbwheel are disabling switches which may be used to ignore any section. The above examples are assuming that the format counters are programmed to reset to the count of zero.

3.4 Preliminary Setup

In order to set up the 4001 PCM System for operation proceed as follows:

a. Turn the ON/OFF switch to the ON position.

b. Select a program card containing the appropriate format. On the 4001 PCM System place the programming lock handle in the down position. Insert the card with the cut edge on the forward left hand side of the slot. Push the card until the locking handle automatically resets (up) and the PROGRAM lamp lights.

c. Set the front panel controls as follows:

1. NORM/INV	NORM
2. WIDE/NAR	Set in accordance with the nature of the input data.
3. OPER/SET	SET
4. MAIN FRAME STRATEGY	All zeros.
5. SELECTED CHANNEL	Set to the word which is under examination.

d. Depress the RESET switch (format sync section) and verify that the appropriate sync status indicators go to SEARCH and return to LOCK.

e. Place a digital voltmeter to the SELECT monitor point on the front panel and adjust R35 (bottom potentiometer) on the D/A converter (card 21) for -2.5 VDC ±10 MV.

f. Place the OPER/SET switch to OPER, and depress the RESET switch on the format sync section. Verify that the appropriate sync status indicators go to SEARCH and return to LOCK. The meter should be in the lower left area of its range.

g. Connect the data to be decommutated to J5. The 4001 PCM System is now ready for operation.

3.4.1 Operating Procedure

As the data is being decommutated by the 4001 PCM System various channels of interest may be monitored by dialing in the appropriate channel on the SELECTED CHANNEL switches. The meter located in the Select and Monitor section will indicate the analog value of the selected channel in percentage of full scale analog output. The meter located in the Bit Synchronizer Section indicates the input data signal quality when the OPER/SET switch is in OPER. Adjustments may be performed to the VCO frequency during decommutation by placing the OPER/SET switch to SET, and adjusting the ADJ FREQ potentiometer for a maximum reading of the meter.

3.5 PROGRAMMING

Programming the 4001 PCM System consists of adjusting the front panel controls and punching a FORMAT STORAGE CARD so as to configure the system to decommutate the specific PCM data of interest. The effects of the various front panel controls are given in Table 3-1.

When a hole is punched in any particular position on the FORMAT STORAGE CARD and the card inserted in the card reader, two contacts, one of which is at ground, the other connected to some logic circuit and at a potential of 5 V DC (thru same impedance), are brought together. Both contacts are then at ground potential and the overall effect is the application of a logical "0" to the circuitry connected with the position. Conversely,if no hole is punched over the position,the contacts are insulated by the card material, a ground is not applied and a logical "1" remains in the circuitry. Since a logical "1" is used as an enabling signal programming the FORMAT STORAGE CARD will generally consist of punching out the undesired particulars of the format. The FORMAT STORAGE CARD contains 12 rows and 22 columns for a total of 264 positions. The function and programming details of each position is described below, and the card layout is shown in Figure 3-5.

A. SYNC CODE - Row 12, columns 1 thru 4 (12-1 thru -4) - These positions are used to define the type of synchronization code employed in the data. The applied codes may be frame synchronization, frame code complement (FCC), frame alternating complement (FAC), unique recycling (URC) and sub-frame identification (SFID). In order to specify a specific sync code holes must be punched over each position which does not apply. FAC for example, is specified by punching holes over positions 12-1, 12-3 and 12-4. Frame synchronization is defined by punching holes in all positions, 12-1 thru 12-4. Since a hole is a logical "0" and no hole is a logical "1", the sync codes are chosen as follows:

	12-1	12-2	12-3	12-4
Frame Synchronization:	0	0	0	0
FCC:	1	0	0	0
FAC:	0	1	0	0
URC:	0	0	1	0
SFID:	0	0	0	1

B. PCM CODE - 12-5 thru 12-10 - These positions are used to specify the data input code to the code converter. The necessary programming for each code is as follows:

	12-5	12-6	12-7	12-8	12-9	12-10
Input Code:	A	B	C	D	D	E
Bi-Phase:	1	0	1	0	1	1
$\overline{\text{Bi-Phase}}$:	1	0	1	1	0	1
RZ:	1	0	1	0	1	0
$\overline{\text{RZ}}$:	1	0	1	1	0	0
NRZ-L:	0	0	0	0	1	0
$\overline{\text{NRZ-L}}$:	0	0	0	1	0	0
NRZ-M:	0	1	1	0	1	0
NRZ-S:	0	1	1	1	0	0

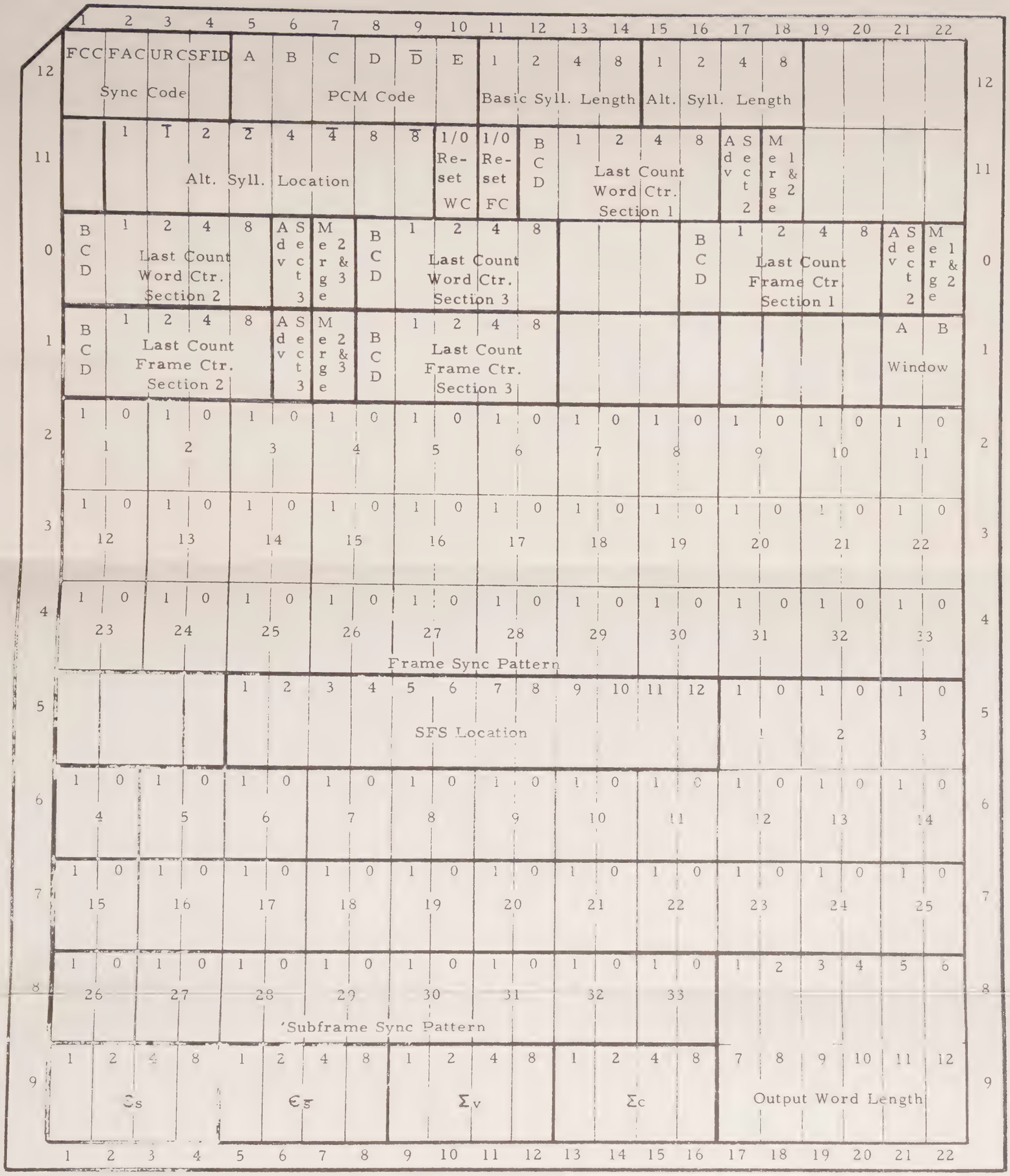
C. BASIC SYLL LENGTH - 12-11 thru 12-14 - These locations are used to define the word length (or basic syllable length if syllabilization is employed) of the data being processed. The length is programmed binarily. The last count of the word is programmed, not the absolute number of bits per word. In the 4001 PCM System, the first count of the bit counter is 0000, hence, the last count of an eight bit word would be 1110 (decimal 7). Note that the most significant bit is to the right.

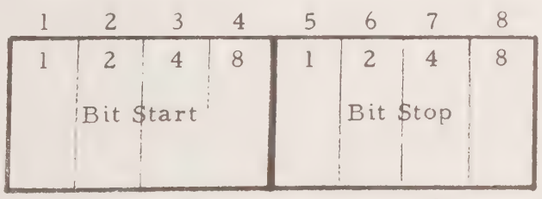
D. ALT SYLL LENGTH - 12-15 thru 12-18 - These locations are used to define the alternate syllable length of the data being processed. The use of syllabilization to increase the basic capabilities of the 4001 PCM System is discussed in a later paragraph. The alternate syllable length is programmed in the same manner as the basic syllable length. However, if an alternate syllable is not to be used program all positions to a "1" (no punch).

E. Blank - 12-19 thru 12-22 - These positions are not used in the programming of the 4001 PCM System.

F. Blank - 11-1 - This position is not used in the programming of the 4001 PCM System.

G. ALT SYLL LOCATION - 11-2 thru 11-9 - These positions are used to define the word in which the alternate syllable is located (refer to paragraph 3.5.2). They determine the count in the


FCC FAC URCSFID
Sync Code
A B C D D̄ E
PCM Code
1 2 4 8
Basic Syll. Length
1 2 4 8
Alt. Syll. Length
1 1̄ 2 2̄ 4 4̄ 8 8̄
Alt. Syll. Location
1/0 Reset WC
1/0 Reset FC
BCD
1 2 4 8
Last Count Word Ctr. Section 1
Adv Sect 2
Mel & ge 2
Last Count Word Ctr. Section 2
Adv Sect 3
Mel & ge 3
Last Count Word Ctr. Section 3
Last Count Frame Ctr. Section 1
Last Count Frame Ctr. Section 2
Last Count Frame Ctr. Section 3
A B
Window
1 0
1 2 3 4 5 6 7 8 9 10 11
Frame Sync Pattern
1 2 3 4 5 6 7 8 9 10 11 12
SFS Location
1 2 3 4 5 6 7 8 9 10 11 12 13 14
'Subframe Sync Pattern
1 2 4 8
Cs
Cs̄
Σv
Σc
7 8 9 10 11 12
Output Word Length



These punch locations are used to select the bit stop & bit start times when format contains SFID. Bit 1→N.

Figure 3-5. Format Storage Card

in the format counter (word) at which the bit counter will count to the alternate syllable length rather than to the basic syllable length. Since it may be required to count to the alternate syllable length every nth word; it is necessary to specify the alternate syllable location so that a "don't care" function may be added. This is accomplished by reading both the Q and $\overline{Q}$ side of the word counter flip-flops and specifying both on the FORMAT STORAGE CARD. Two "0"s are then used to ignore more significant counting stages. To program the alternate syllable location proceed as follows:

1. Determine the alternate syllable position, for example, syllable 5.
2. Program this position binarily on the true positions (1, 2, 4, 8) and the complement of this number in the $\overline{\text{true}}$ positions ($\overline{1}$, $\overline{2}$, $\overline{4}$, $\overline{8}$)
3. Program "0" in all positions corresponding to rates slower than desired. The program for an alternate syllable location of syllable 5 is 10011000. Note that the most significant bit is to the right.

If an alternate syllable is not being used, program all lines high ("1"), i.e. no punch.

H. RESET WC - 11-10- This position is used to determine whether the first group of format counters (word) are reset to the count

of 0 or reset to the count of 1. To reset to "0", program a "1" (no hole); to reset the counter to "1" program a "0". The count to which the frame counters are reset is preferential, but once chosen; affects the word identification and last count frame programs.

NOTE: It is important to realize that a reset to "1" deletes the "0" count from the first group of counters unless the "MERGE" function is being planned.

I. RESET FC - 11-11 - This position is used to determine whether the first group of frame counters are reset to the count of "0" or reset to the count of "1". To reset a "0" program a "1" (no hole); to reset the count to "1" program a "0". The count to which the frame counters are reset is preferential but once chosen will affect the word identification and last count frame.

NOTE: It is important to realize that a reset to "1" deletes the "0" count from the first group of counters unless the "MERGE" function is being planned.

J. BCD - 11-12 - This position, used in conjunction with the LAST COUNT WORD CTR, Section 1, determines whether the word counter output will be a binary or binary coded decimal (BCD) identification. If a binary is desired, program a 0; if BCD is desired program a 1.

K. LAST COUNT WORD COUNTER, SECTION 1 - 11-13 thru 11-16 - These positions are used to program the last word count of the frame. This section is a 4 stage binary counter which may be used alone or in conjunction with Sections 2 and 3 to define the

last word count of the frame from between 0 to 4096. The counter may be configured to count in any base although it is always programmed binarily. To program the LAST COUNT WORD COUNTER, SECTION 1, program binarily remembering that the last count will be the counter cycle length if the counters are reset to 1 or counter cycle length minus one of the counters are reset to zero. The reset will be identification for the first word in the frame sync pattern. Note that the most significant bit is to the right.

L. ADV SECTION 2 - 11 -17 - This position gates the last count of Section 1 to Section 2. This effectively connects the two sections serially. To make this conversion program a 1.

M. MERGE 1 & 2 - 11 -18- This position inhibits the resetting of LAST COUNT WORD COUNTER, SECTION 1, on the count programmed and allows the overall last count of Sections 1 and 2 to be programmed as one total count. For instance, to program a last count of 21, a 5 stage word counter is needed and the last count programmed as 10101. To accomplish this ADV SECT 2 is programmed high configuring the eight stages sequentially and since Section 1 must be prevented from resetting on 10100, Merge 1 & 2 is programmed high (1 to merge, 0 to not merge). Note that the most significant bit is to the right. When the merge function is activated the first section will count to its maximum count

and reset to "0" until the total last count for the two sections is reached. At this time the first group will reset to "1" or "0" as programmed in H. If any group of counters is not to be programmed, punch out all punch areas. (Program all "0"s.)

N. Blank - 11-19 thru 11-22 - These positions are not used in the programming of the 4001 PCM System.

O. BCD - 0-1 - This position, used in conjunction with the LAST COUNT WORD COUNTER, SECTION 2, determines whether the word counter output will be a binary or binary coded decimal. If a binary decimal output is to be used program a "1"; all other cases program a "0".

P. LAST COUNT WORD COUNTER, SECTION 2 - 0-2 thru 0-5 - This section is used to program the last word count of the frame. This section is a 4 stage binary counter which may be used in conjunction with Sections 1 and 3 to define the last word count of the frame from between 0 to 4096. The counter may be configured to count in any base although it is always programmed binarily. To program the LAST COUNT WORD COUNTER, SECTION 2, program binarily remembering that the last count in combination with Section 1 will be the counter cycle length if the counters are reset to 1, counter cycle length minus 1 or if the counters are reset to zero. If this section is used as part of a binary counter the last count is programmed using Sections 1 and 2; or Sections 1, 2 and 3, as the case may be, as an 8 and 12 stage counter, respectively.

Q. ADV SECTION 3 - 0-6 - This position gates the last count of Section 2 to Section 3 converting from a 4 stage to an 8 stage counter (or from an 8 to a 12 stage counter). To make this conversion program a "1".

R. MERGE 2 & 3 - 0-7 - This position inhibits the resetting of LAST COUNT WORD COUNTER, SECTION 2, on the count programmed and allows the overall last count of Sections 2 and 3 to be programmed or 1, 2, & 3 as the case may be. For instance, to program a last count of 300 a 9 stage word counter

is needed and the last count programmed as 001101001. To accomplish this ADV SECT 1 & ADV SECT 2 are programmed high ("1") configuring the 12 stages sequentially;and since Sections 1 and 2 must be prevented from resetting until the total last count is reached. Merge 1 & 2 and Merge 2 & 3 is programmed high ("1" to merge, "0" to not merge). Note that the most significant bit is to the right.

S. BCD - 0 - 8 - This position, used in conjunction with the LAST COUNT WORD COUNTER, SECTION 3, determines whether the word counter output is a binary coded decimal. If a binary output is to be used, program a "0"; if a binary coded decimal is to be used, program a "1".

T. LAST COUNT WORD COUNTER, SECTION 3 - 0-9 thru 0-12 - These positions are used to define the last count of the word counter, Section 3. The last count is programmed similarly as Sections 1 and 2.

U. Blank - 0-13 thru 0-15 - These positions are not used in the programming of the 4001 PCM System.

V. BCD - 0-16 - This position, used in conjunction with the LAST COUNT FRAME COUNTER, SECTION 1, determines whether the frame counter output will be a binary or binary coded decimal. If a binary output is to be used program a "0"; if a binary coded decimal is to be used,program a "1".

W. LAST COUNT FRAME COUNTER, SECTION 1 - 0-17 thru 0-20 - This group is used to program the last count of the first section of the frame counter. This section is a 4 bit counter which may be used alone or in conjunction with Sections 2 and 3 to define the last frame count from between 0 to 4096. The counter may be configured to count in any base although it is always programmed binarily. To program the LAST COUNT FRAME COUNTER, SECTION 1, program binarily remembering that the last count will be equal to the counter cycle length if the counters are reset to 1; or cycle length (1) if the counters are set to zero. Note that most significant bit is to the right.

X. ADV SECTION 2 - 0-21 - This position gates the last count of Section 1 to Section 2 converting from a 4 stage to an 8 stage counter. To make this conversion program a "1".

Y. MERGE 1 & 2 - 0-22 - This position inhibits the resetting of LAST COUNT FRAME COUNTER, SECTION 1, on the count programmed and allows the overall last count of Sections 1 and 2 to be programmed as one total count. For instance, to program a last count of 21 a 5 stage frame counter is needed and the last count programmed as 10101. To accomplish this ADV SECT 2 is programmed high configuring eight stages sequentially;

and since the Section 1 must be prevented from resetting on 10100; MERGE 1 & 2 is programmed high ("1" to merge, "0" to not merge). Note that the most significant bit is to the right.

Z. BCD - 1-1 - This position, used in conjunction with the LAST COUNT FRAME, SECTION 2, determines whether the frame counter output will be a binary or binary coded decimal. If a binary coded decimal output is to be used, program a "1"; in other cases program a "0".

a. LAST COUNT FRAME COUNTER, SECTION 2 - 1-2 thru 1-5 - This section is used to program the last frame count of the subframe. This section is a 4 bit counter which may be used in conjunction with Sections 1 and 3 to define the last word count of the subframe from between 0 to 4096. The counter may be configured to count in any base although it is always programmed binarily. To program the LAST COUNT FRAME COUNTER, SECTION 2, program binarily, remembering that the last count is equal to the counter cycle length if the counters are reset to 1; or counter cycle length - 1, if the counters are set to zero.

b. ADV SECTION 3 - 1-6 - This position gates the last count of Section 2 to Section3 converting from a 4 stage to an 8 stage counter (or from an 8 to a 12 stage counter). To make this conversion program a 1.

c. MERGE 2 & 3 - 1-7 - This position inhibits the resetting of LAST COUNT FRAME COUNTER, SECTION 2, on the count programmed and allows the overall last count of Sections 2 and 3 to be programmed. For instance, to program a last count of 300 a 9 stage frame counter is needed, and the last count programmed as 001101001. To accomplish this ADV SECTION 2 is programmed high, to configure the 12 stages sequentially and since Sections 1 & 2 must be prevented from resetting until the total count is reached, Merge 1 & 2 is programmed high (1 to merge, 0 to not merge). Note that the most significant bit is to the right.

d. BCD - 1-8 - This position, used in conjunction with the LAST COUNT FRAME COUNTER, SECTION 3, determines whether the frame counter output will be a binary or binary coded decimal. If a binary output is to be used program a 0; if a binary coded decimal is to be used program a 1.

e. LAST COUNT FRAME COUNTER, SECTION 3 - 1-9 thru 1-12 - These positions are used to define the last count of the frame counter, Section 3. The last count is programmed similarly as Sections 1 & 2.

f. Blank - 1-13 thru 1-16 - These positions are not used in the programming of the 4001 PCM System.

g. Blank - 1-17 thru 1-20 - These positions are not used in the programming of the 4001 PCM System.

h. WINDOW - 1-21 & 1-22 - These positions define the window length and hence, the aperture of the correlator. Program binarily according to the desired length as follows.

Program	Window Length
00	1 bit
10	3 bits
11	5 bits

i. FRAME SYNC PATTERN - 2-1 thru 4-22 - The specific frame synchronization pattern is programmed in these positions. There are two positions for each sync bit: program a 10 when the sync bit is to be a "1", program 01 when the sync bit is to be a "0", program 11 for bit positions not part of the sync pattern, that is, a 11 program is a "don't care" function, and is used in the last "n" positions when the sync pattern length is 33 - n bits long).

j. Blank - 5-1 thru 5-8 - These positions are not used in the programming of the 4001 PCM System.

k. SFS LOCATION - 5-5 thru 5-16 - These positions are used to locate the subframe sync pattern (SFID or URC) within the main frame (when used). The first word in which the sync pattern is located is programmed binarily, in accordance with the radix to which the counters have been configured. That is, if the 3 sections of the word counters have been configured as a BCD counter than the SFS location must be programmed as a binary coded decimal. The designators 1 thru 12 indicate the counting stages of the word counter.

l. SUBFRAME SYNC PATTERN - 5-17 thru 8-16 - The specific subframe synchronization pattern is programmed in these positions. There are two positions for each sync bit; program a 10 when the sync bit is to be a 1, program 01 when the sync bit is to be a 0, program 11 for bit positions not part of the sync pattern (that is, a 11 program is "don't care" function and is used in the last n positions when the sync pattern length is 33-n bits long).

m. OUTPUT WORD LENGTH - 8-17 to 8-22, 9-17 to 9-22 - The output word length of the 4001 may vary from 0 to 12 bits and these positions are programmed to determine what this length shall be. The positions are numbered according to stages of

the storage register from 1 (MSB) to 12 (LSB). For word lengths shorter than 12 bits punch out undesired stages.

o. e_s - 9-1 thru 9-4 - Error tolerance control for subframe sync patterns in SEARCH. Program binarily from 0 to 9 only. Note that the most significant bit is to the right.

p. $e_{\bar{s}}$ - 9-5 thru 9-8 - Error tolerance control for subframe sync patterns in $\overline{\text{SEARCH}}$. Program binarily from 0 to 9 only. Note that the most significant bit is to the right.

q. Σ_V - 9-9 thru 9-12 - VERIFY accumulator control for subframe synchronization. Program binarily from 0 - 15. Note that the most significant bit is to the right.

r. Σ_c - 9-13 thru 0-16 - CHECK accumulator control for subframe synchronization. Program binarily from 0 - 15. Note that the most significant bit is to the right.

s. BIT START - 8-1 thru 8-4 - These locations are used to select the bit start times when the format contains SFID. Program binarily. Note that the most significant bit is to the right.

t. BIT STOP - 8-4 thru 8-8 - These locations are used to select the bit stop times when the format contains SFID. Program binarily. Note that the most significant bit is to the right.

3.5.1 Word and Frame Counter Radices

The word and frame counters when installed consist of 3 sections, each section containing a four stage counter. Thru the use of the LAST COUNT, ADVANCE AND MERGE positions on the FORMAT STORAGE CARD, the 12 counting stages may be configured to count to any desired radix. The most commonly used are the base 2 and the base 10. The radix that is employed is usually dictated by the sample ratio in the format or by the requirements of some peripheral equipment such as DCS Word Selectors. When configuring these counters you must remember two basic requirements:

a. The counter programs must be consistent.

b. The counter operation must be compatible with the requirements of peripheral equipment.

The requirement of program consistency requires that all programs directly affected by the frame or subframe counters be programmed to the same radix in which the counters are operating. Although this applies directly to the operation of word selectors, display units, and other equipments into which the 4001 PCM System is operating, it is of chief concern here when programming the subframe sync location, the selection of words for display on the Select and Monitor Section (SELECTED CHANNEL switches) and the use of the SPECIAL WORD LOCATION switches in the simulator section.

Compatibility is best assured with peripheral equipment by an investigation of input requirements to these devices. If the PCM data

contains supercommutated channels for instance, word selectors will require word identification data coded in a binary coded variable radix where the radices are equivalent to the supercommutation ratios. This becomes an operating requirement on the 4001 PCM System since the word identification is the word and frame counter outputs.

3.5.2 Syllabilization

Data words may be syllabilized to increase the efficiency of transmission or to increase the capabilities of the 4001 PCM System. In the former case the syllabilization is performed in the remote location and generally a syllable contains a whole piece of channel information (measurand). On the other hand the word length capability of the 4001 may be increased by breaking the basic word into syllables. In either case the programming is similar and is best illustrated by an example:

Consider a format in which the word length is 27 bits. Since the maximum count in the bit counters is 15 (16 counts) it may appear to be beyond the system's capacity to handle at first glance. However, if we redefine the word length (BASIC SYLLABLE LENGTH) to 8 bits, one format word will consist of 8-8-8-3 bits or 3 basic syllables of 8 bits and one alternate syllable of 3 bits located in redefined word 4 (ALTERNATE SYLLABLE LOCATION) and may be programmed accordingly.

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section describes the principles of operation of the 4002 PCM System.

4.1.1 Definitions

Although the majority of PCM terms and definitions in use today are industrial standards there are some which are peculiar to each facility. To avoid ambiguity resulting from undefined terms, a glossary of terms and definitions used in this instruction manual is given in Section VI.

4.1.2 Logic

The 4001 PCM System is an all solid state device employing both transistors and integrated circuit logic (IC). The IC devices are Texas Instrument 74N series transistor-transistor-logic (TTL) or diode transistor logic (DTL) series 15N. A logical "1" sometimes called a true or high level, is a nominal +3.2 VDC although this value may vary from +2.5 to +5.5 VDC. A logical "0" also called false or low level, is nominal 0 VDC which may vary between 0 VDC and +0.4 VDC from component to component.

4.2 FUNCTIONAL DESCRIPTION

Figure 4-1 is a functional block diagram of the 4001 PCM System illustrating the manner in which PCM data is decommutated. Input data of any format is applied to the bit synchronizer which accepts a noisy unbalanced and unstable input and presents a reconstructed output, synchronous with a bit rate clock generated in the synchronizer. The data is regenerated through the use of an internal voltage controlled oscillator which is phase locked to the input data.

The reconstructed data presented at the output of the bit synchronizer remains in the same format (NRZ, RZ, Bi-Phase) as the data applied. The format synchronizer contains a code converter shift register, storage register, format counter and correlator circuits which are used in the decommutation and synchronization process. The code converter by standardizing all input codes to NRZ-L simplifies the necessary programming in the balance of the system.

The shift register is used to convert from serial to parallel data. Each data bit is shifted into the shift register on every clock cycle (derived from the VCO output of the bit synchronizer). A data word, therefore, will appear in its proper location for only one clock cycle which is insufficient time to guarantee word selection, D/A conversion, and application to computer, etc. The parallel data is transfered to the storage register where each word remains for one word length. Transfer synchronization, that is, the dumping of parallel data into the storage register from the shift register, must occur only at the precise moment the entire word is located in the correct stages, and all stages are settled. This is accomplished by programming and is based on a foreknowledge of the incoming data word length, frame length, etc.

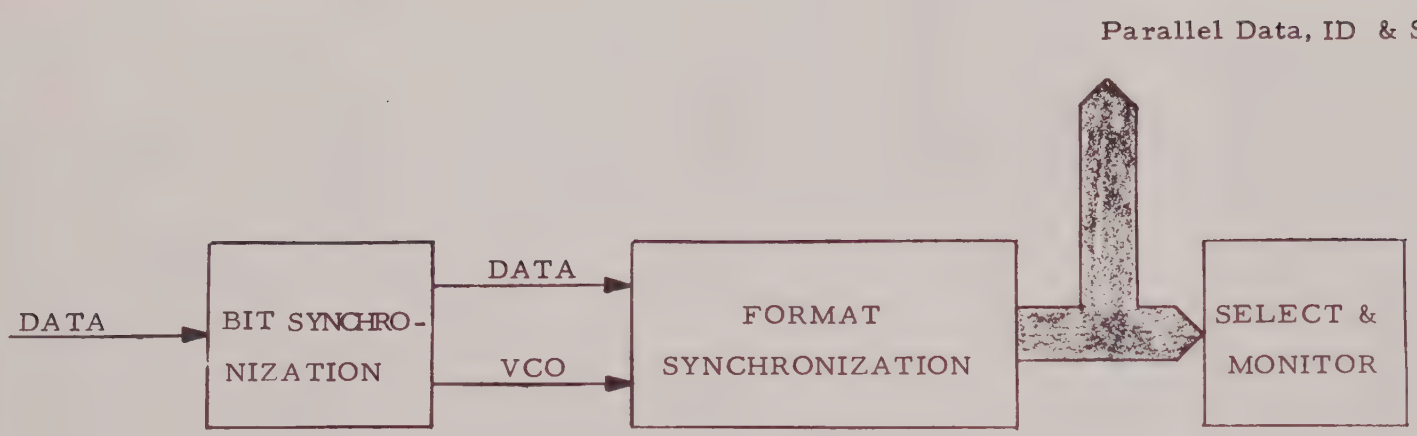


Figure 4-1. Block Diagram, 4001 PCM System

The output of the storage register is available at the output of the 4002 PCM System where it may be applied to a computer, multi-channel word selector or other readout devices. A single channel word selector is supplied with the system which is capable of selecting any specific word in a format for binary displays D/A conversion and meter display.

In order to properly decommutate PCM data it is extremely important that the clock frequency generated in the bit synchronizer be synchronous with the clock frequency used in the commutation process at the remote location. In addition, words and frame must be identified. This is accomplished by the use of synchronization patterns of up to 33 bits. These synchronization patterns are used as reference points from which words and frames are located. As data is shifted into the shift register a pattern recognizer looks for this synchronization code in the proper location in the register. When it appears, a pulse is applied to the correlation circuits and a counting sequence initiated. There are up to three counters in the 4001 PCM System driven by the bit synchronizer clock; a bit counter, word counter, and frame counter (Model 4001-100, -110, -111). The outputs of these various counters are used as word identification signals in the word selection devices.

4.3 4001 PCM SYSTEM FUNCTIONAL UNITS

From a remote location such as a satellite or locally from a tape recorder, serial pulse code modulated data is applied to the 4001 PCM System. The system accepts this data and performs a number of intermediate operations in order to give a 12 bit parallel data output with accompanying identification. These intermediate operations are:

a. Bit Synchronization

b. Code Conversion

c. Registration

d. Storage

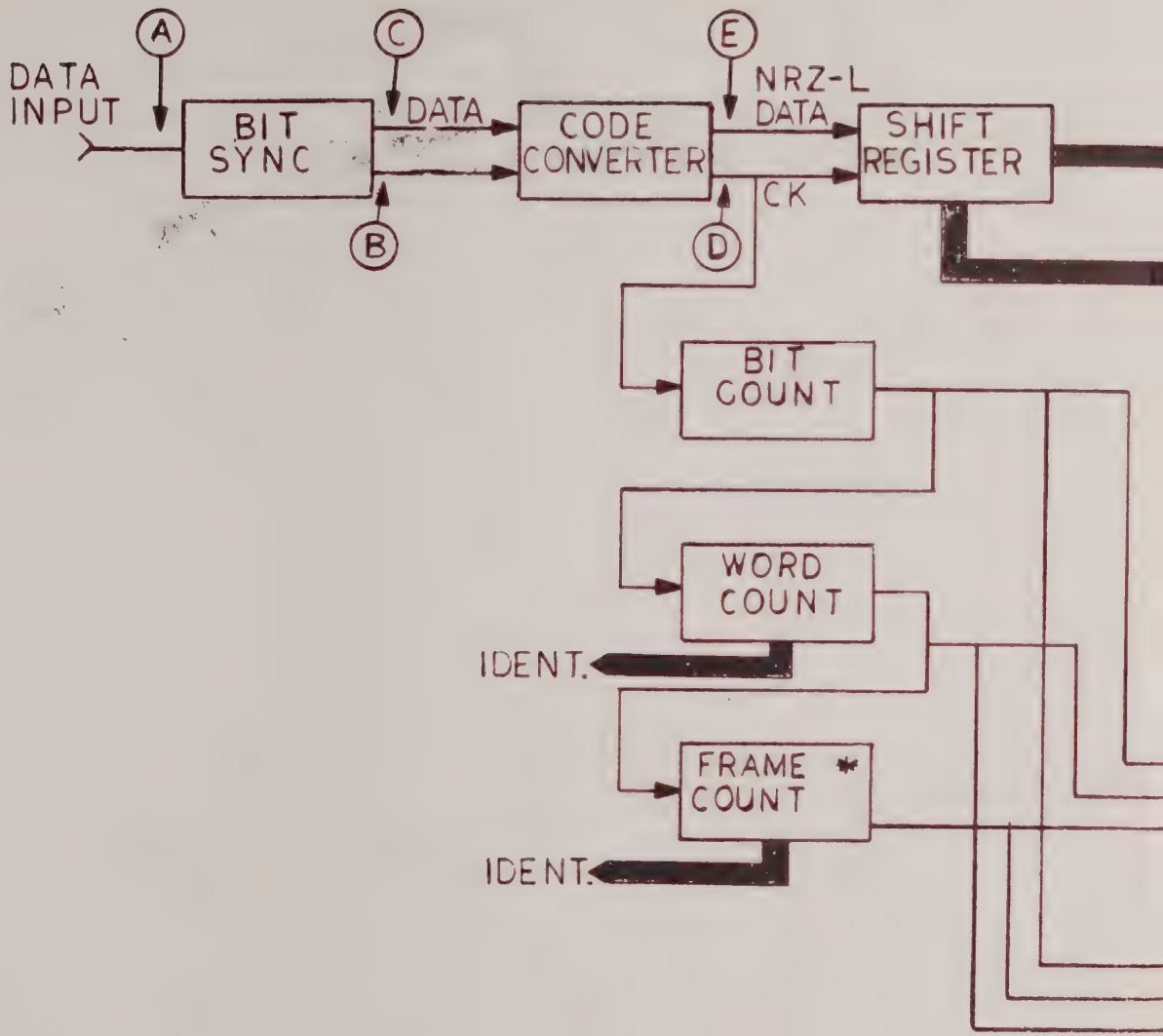
e. Digital-to-Analog Conversion (for selected analog output)

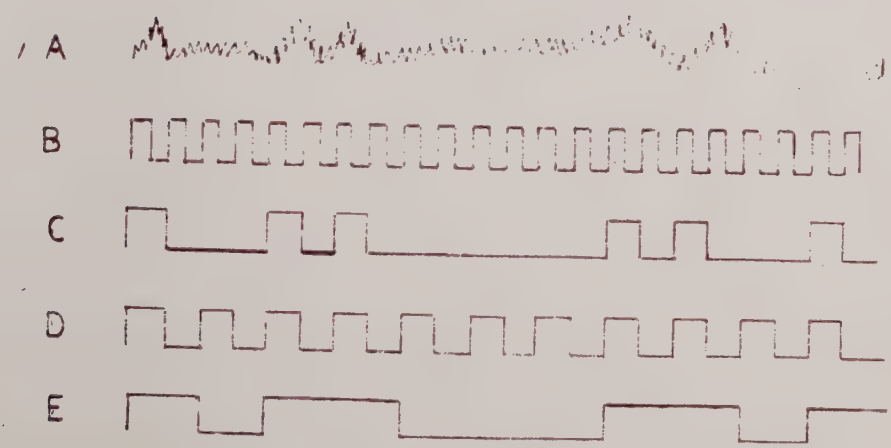
An important corollary operation performed by the system as this data is being processed is the maintenance of synchronization, timing and word, frame, and channel identification of all data contained in the registration and storage sections. Figure 4-2 is an expanded block diagram of the 4001 PCM System illustrating these functions. For illustrative purposes, an RZ code is assumed to be applied.

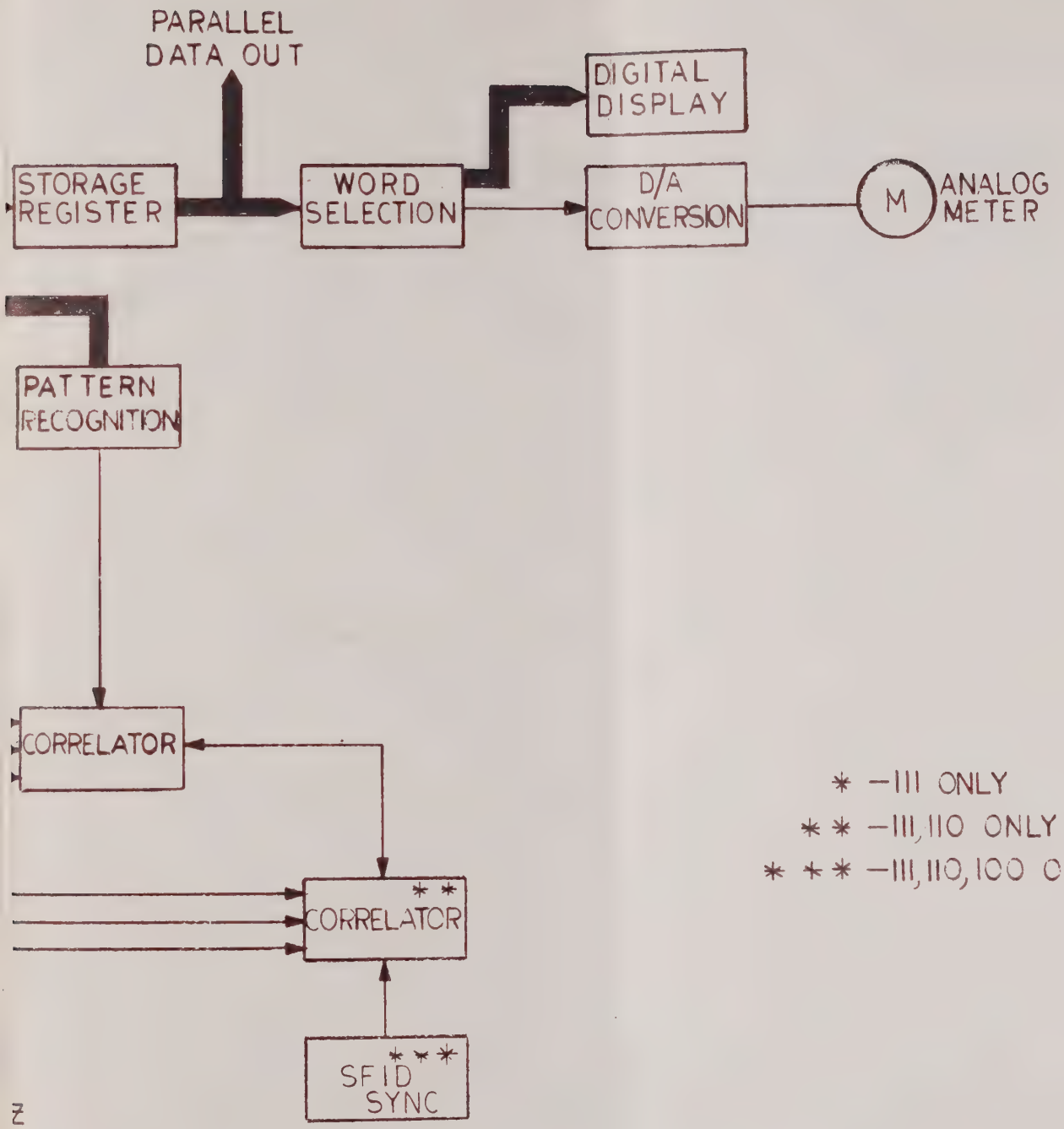
4.3.1 Bit Synchronization

Data applied to the system is supplied with no timing signals other than a synchronization code and usually degraded as illustrated. Initially, a clean PCM signal is generated but distance and signal conditioning add background noise, DC unbalance (baseline gallop), and jitter.

The function of bit synchronization is to generate a valid synchronous clock which may be used as a basic timing signal throughout the balance of the PCM System and to detect each bit of data, reconstruct it, and supply clean data to the code converter. Bit synchronization is accomplished in the 4001 PCM System with a plug-in modularized bit synchronizer (DCS Model SBS-2). Located in the first seven slots of the card file, this unit employs a phase lock loop to accomplish necessary timing and clock generation. The nominal bit rate is determined by a preselected plug-in tuning unit which operates through a given range, (Table 1-1). The


A
C
E
DATA
INPUT
BIT
SYNC
DATA
CODE
CONVERTER
NRZ-L
DATA
SHIFT
REGISTER
CK
B
D
BIT
COUNT
WORD
COUNT
IDENT.
FRAME *
COUNT
IDENT.


A
B
C
D
E



* —111 ONLY
* * —111, 110 ONLY
* * * —111, 110, 100 ONLY

Z

CO

Z

LOCK

RZ-L

DETAILED
BLOCK DIAGRAM
4001 PCM SYSTEM
FIG 4-2

timing signals presented to the code converter are in all cases except for RZ and Bi-Phase data the basic system clock. When RZ or Bi-Phase data is applied to the system the bit synchronizer will present a timing signal of two times the system clock (2CK) to the code converter where it is divided by 2 prior to use in the balance of the system.

4.3.2 Code Conversion

In order to allow the 4001 PCM System to decommutate diverse types of data, a code converter has been installed which standardizes all PCM input codes to NRZ-L.

FORMAT STORAGE CARD locations 12-5 thru 12-10 are used to reduce the general circuitry of the code converter to an equivalent circuit suitable to convert the specific code applied. The following correlates the applied codes and their programs.

Input Code	Program
NRZ-L	000100
NRZ-M	011100
NRZ-S	011010
RZ	101100
Bi-Phase	101101
Inverted Bi-Phase	101011
Inverted NRZ-L	000010
$\overline{\text{RZ}}$	101010

4.3.3 Shift Register

The serial output data from the code converter is applied to a shift register. This register contains 33 stages and is suitable for synchronization patterns up to this length. Since only the outputs of 12 stages are applied to the storage registors, output word length is limited to 12 bits without syllabilization. The shift register is a standard logic configuration with system clock used to transfer data bits from stage to stage; a word strobe pulse rising when a

complete word is in proper location, is used to load the data to parallel storage. Hence, the application of this shift register is as a serial to parallel data converter.

4.3.4 Storage Register

The storage register is used to store parallel data for one word length, the contents of which are data values of one channel. Each output of the storage register is brought to the rear connector panel where they are available for application to data reduction devices. Each output is also applied to the select and monitor subsystem where any desired channel may be selected and displayed. The storage register contains 12 stages and will store words up to this length. Shorter word lengths are accommodated by disabling unused stages which is accomplished through programming (OUTPUT WORD LENGTH 1-12, positions 8-17 thru 8-22, and 9-17 thru 9-22 on the FORMAT STORAGE CARD).

4.3.5 Word Selection and Display

Any word contained in the PCM data applied to the system may be selected and displayed on the front panel. The output data contained in the storage register is also applied internally to a digital storage register; and from there to a digital-to-analog converter. Word identification signals are used to identify the desired word through thumbwheel programming. The digital value contained in the storage register is also displayed binarily.

4.3.6 Synchronization and Identification

PCM data can not be decommutated without a reference from which individual frames and words can be identified, hence it is necessary that the storage registers be loaded only when a complete word is loaded in the shift register. This reference is the synchronization

discretion of the operator.

When the system is operating in the LOCK mode synchronization is maintained, and since the sync pattern is being scanned only at the time at which it is expected the danger of recognizing data as a sync pattern is eliminated.

If the sync pattern should not appear at the expected time, the system is immediately placed in the CHECK mode where it will remain while the decision is made as to whether or not synchronization is being maintained. One sync pattern occuring at the expected time will revert the system to LOCK. A selected number of sequentially incorrect patterns will place the system in the SEARCH mode where the process of acquiring LOCK is repeated. The number of successive incorrect patterns necessary for this is determined by front panel mounted thumbwheel and may vary from 0 to 15 at the discretion of the operator. The status of the system is displayed on indicator lamps on the front panel.

The second source of synchronization error in any PCM decommutator arises from failing to recognize a synchronization pattern because of bit errors. Front panel thumbwheel switches and allows the selection of from 0 to 9 errors in the sync pattern while in the SEARCH mode or the $\overline{\text{SEARCH}}$ mode and still be recognized. Two switches are provided allowing two different choices, since the danger of recognizing data as a sync pattern is considerable reduced in the $\overline{\text{SEARCH}}$ modes of operation.

4.3.8 Subframe Synchronization

The preceding paragraphs on the signal flow and synchronization of the 4001 PCM System described the decommutation methods employed

on all standard models of the 4001 series. The list of these standards and their additional capabilities are:

4001-000	Frame Synchronization
4001-100	Frame Code and Frame Alternating Complement Synchronization
4001-110	Frame Code, Frame Alternating Complement and Unique Recycling Synchronization
4001-111	Frame Code, Frame Alternating Complement, Unique Recycling and Subframe identification word Synchronization

Each of these models, except for the 000 Model, contain additional circuits to enable subframe synchronization.

Model 4001-000- This Model PCM System is the basic configuration from which all others are derived. The general principles of operation have been given in preceding paragraphs and the differences between this and succeeding models are illustrated in Figure 4-2.

Model 4001-100- This Model is capable of handling all of the formats of the 4001-000 plus the ability to handle frame code and frame alternating complement synchronization patterns. In order to accomplish this a counter is added to the -000 model (the frame counter of Figure 4-2). The frame length (words per frame) which is programmed on the FORMAT STORAGE CARD is used to determine the last count of the sub-frame. As the word counter is reset at the end of a frame, an advance pulse is applied to the frame counter. Since the count of the frame counter is equivalent to a specific word in the subframe, sub-channel identification is obtained.

These are three subframe operating modes in the -100 model PCM system. SEARCH, LOCK and CHECK which operate in a similar fashion as the main frame operating modes. The synchronization pattern corresponding to the subframe will be the complement of

all other sync patterns. This unique pattern is used as a pattern recognition signal in the FCC correlator which is a part of the main frame correlator assembly. When this signal is coupled with the last count of the frame counter; it is used to evaluate the synchronization of the subframe.

A frame alternating complement synchronization pattern is used to provide additional confidence in main frame synchronization. The complement of the frame synchronization pattern is placed in each alternate frame to prevent lock on repetitive data similar to the sync pattern.

Model 4001-110- This model has all of the capabilities of the 4001-100 plus the ability to handle a unique recycling code. The URC code is a subframe synchronization pattern occuring in a different word than that of the main frame sync pattern. To accommodate the URC code, another correlator and frame counter are added to the basic system. The subframe operating modes are independent of the main frame modes (although the main frame has priority). These modes are SEARCH, VERIFY, LOCK and CHECK. When the main frame sync pattern is recognized, the unit goes to a $\overline{\text{SEARCH}}$ mode (VERIFY, LOCK or CHECK), after which the subframe pattern recognizer is activated, and the second correlator looks for the unique recycling code at the expected word time of each frame. The first recognized subframe code resets the frame counters and advances the subframe correlator to VERIFY. After the frame and/or subframe correlators advance to LOCK absence of the unique recycling code returns the second correlator to CHECK for accumulation of incorrect patterns. If the accumulation reaches the number specified for the subframe strategy the correlator returns to SEARCH mode. The main frame correlator maintains top priority at all times. If the main frame

correlator reverts to SEARCH, the subframe correlator reverts to the same mode. All subframe strategy is programmed via the FORMAT STORAGE CARD.

Model 4001-111- This model has all the capabilities of the 4001-110 plus subframe identification. A PCM format which contains subframe identification utilizes several consecutive bits located within a frame to provide identification of the subframe words. The SFID bits change at the main frame rate usually in a binary count method and is employed to place a unique count within the transmitted data for identification so that subframe word identification may commence immediately within any frame; hence, avoids waiting for a specific pattern at the subframe rate.

Main frame synchronization strategy is identical to the -000 models and maintains first priority over any subframe mode.

The location and configuration of the subframe identification is programmed on the format storage card. The identification may be up to 8 bits and start with 0 or 1; and progressively, increase to any binary number within the limits of eight bits. After the main frame correlator has advanced to VERIFY, the data SFID contained in the correct word position are stored. The frame counters are then updated until the count matches the stored value. At this point, a comparison is made of the data ID value and the SFID value. If the values are identical, the subframe mode transfers to VERIFY and then to LOCK in a similar manner as the main frame modes.

4.3.9 System Timing

The key timing signals and their relationship to a PCM format are shown in Figure 5-1. The period of time illustrated in the diagram is the last two words of a frame and the first two words of the

succeeding frame. Although the number of words per frame are unspecified, an eight bit word length has been shown for simplicity but the relationships shown are independent of word length, e.g. LAST COUNT will always go low on the last clock cycle of the word regardless of length. The nomenclature used for each signal is identical to that used on the block and logic diagrams and a description of each may be found in the glossary.

4.3.10 Programming

All programming performed on the 4001 system is applied to the system via front panel controls or a FORMAT STORAGE CARD. The format storage card is flexible plastic measuring 3.25" x 2.25" and supplies information to the system through the relative positions of punched rectangular holes on its surface. The card is inserted in the card reader (AMP Corp. P/N 426666-3) which translates the hole patterns into electrical signals to supply the programmed information to appropriate gates.

The card reader contains two contacts for each piece of information to be programmed, one of which is at ground while the other is connected to some logic circuitry and is at +5 VDC (thru some impedance). When the format storage card is inserted, a latch is released causing the lock mechanism to actuate, the handle rises and all contacts attempt to close. The program card, however, only allows contact closure where holes are located and prevents closure on all others. Holes, therefore, are equivalent to a logical "0" while no hole is equivalent to a logical "1". It is important to note at this point that most programming information in the 4001 system is applied thru the use of a logical "1" or by not punching a hole over a particular position, i.e. when programming for a particular PCM format holes are punched over those positions which do not apply.

The programming positions and functions of the format storage card are given in Section III.

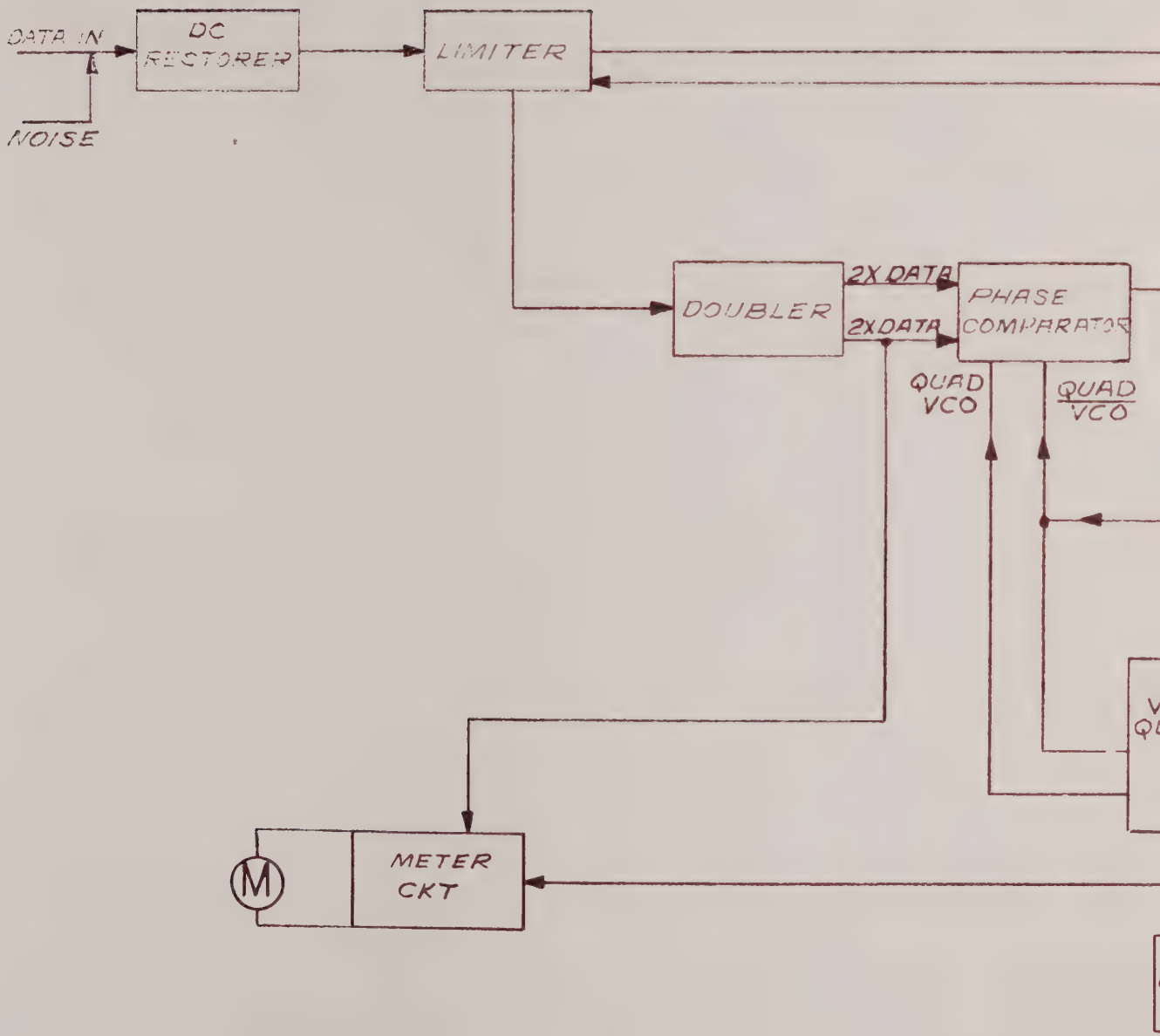
4.3.11 Physical Description

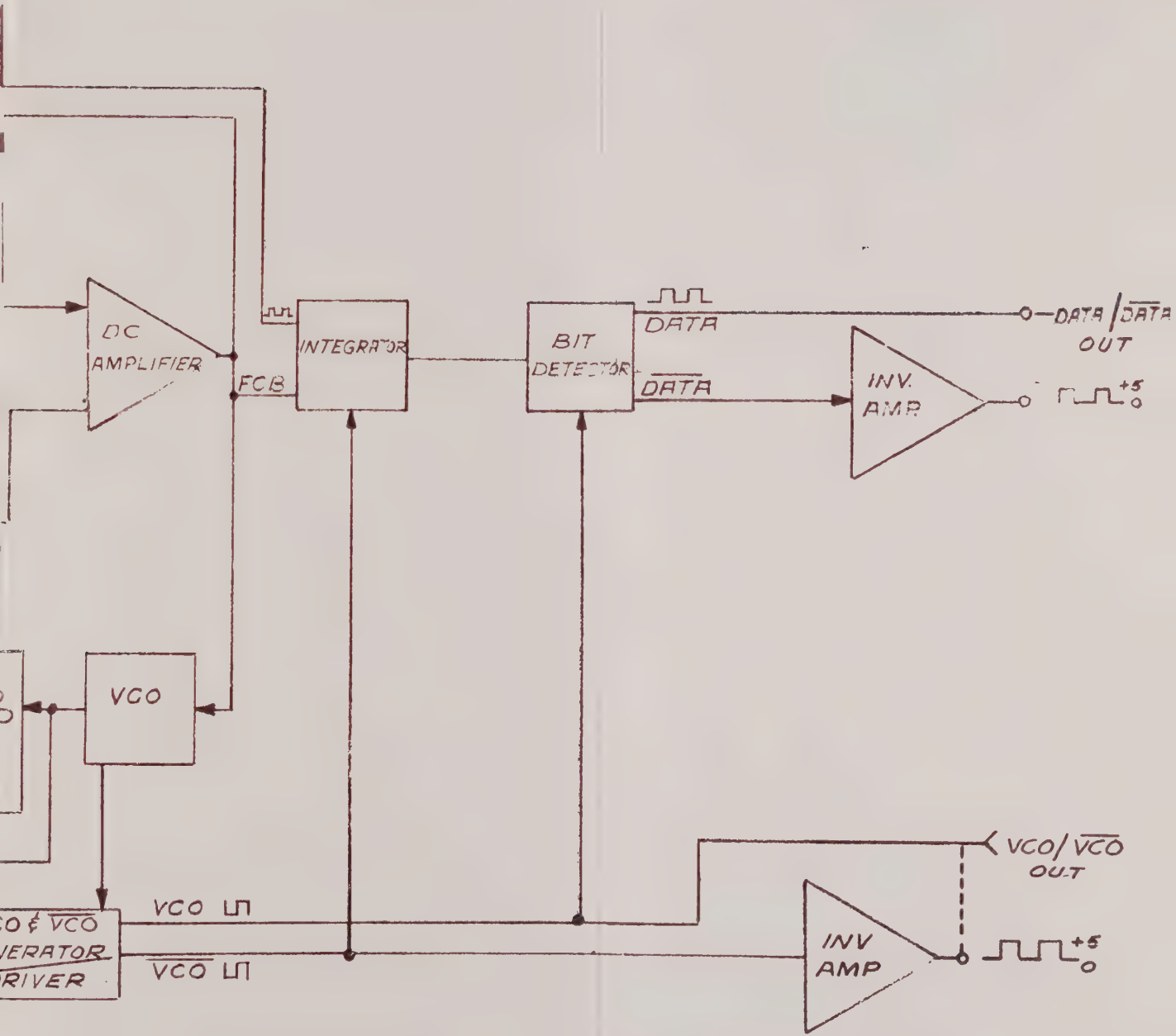
Figure 5-4 is a block diagram of the bit and format synchronizers, and the Select and Display sections of the 4001 PCM system which illustrates the electrical and physical interelationship of the various circuit cards employed to accomplish the control and decommutation of PCM data. The correlation of any particular block Figure 5-4 to a functional block given in Figure 4-2 can be determined by comparing the two diagrams. Two exceptions may be the control logic and the error detector circuit cards. The control logic cards are described in the following paragraphs and are used to accomplish many miscellaneous tasks such as switching, buffering, enabling, disabling, etc., and have no effect on the functional description of the 4001 PCM System. The error detector, although contained on a separate card, is actually part of the Pattern Recognizer.

4.4 SBS-2 BIT SYNCHRONIZER

The input to the bit synchronizer is a noisy, galloping and jittery serial PCM wavetrain similar to the wave shown in Figure 4-2. The SBS-2 evaluates this data, reconstructs and applies to the code converter, a clean wavetrain synchronous with a generated timing signal (VCO). The block diagram of this subsystem is shown in Figure 4-3.

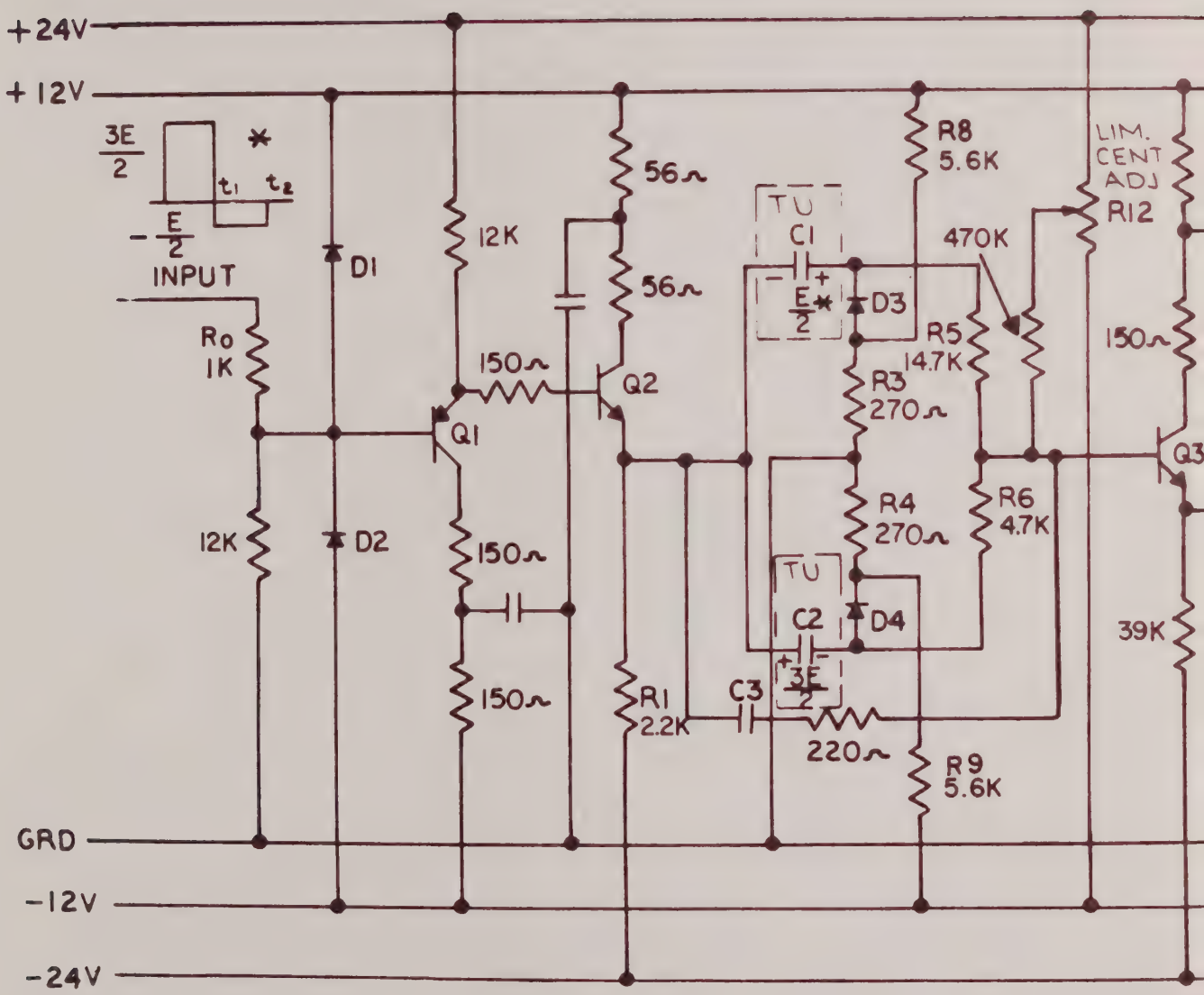
The DC restorer and limiter is used to establish a dc level, eliminating the gallop of the input data. After the dc level is established, the following events take place:


DATA IN
NOISE
DC RESTORER
LIMITER
DOUBLER
2X DATA
2X DATA
PHASE COMPARATOR
QUAD VCO
QUAD VCO
METER CKT
M



FUNCTIONAL BLOCK DIAGRAM
SBS-2 BIT SYNCHRONIZER

FIG. 4-3


+24V
+12V
3E/2
t1
t2
-E/2
INPUT
R0 1K
12K
D1
D2
12K
150Ω
Q1
56Ω
56Ω
Q2
150Ω
150Ω
R1 2.2K
C3
TU
C1
E/2
D3
R8 5.6K
470K
R5 14.7K
R3 270Ω
R4 270Ω
TU
C2
D4
3E/2
220Ω
R9 5.6K
R6 4.7K
LIM. CENT ADJ R12
150Ω
Q3
39K
GRD
-12V
-24V

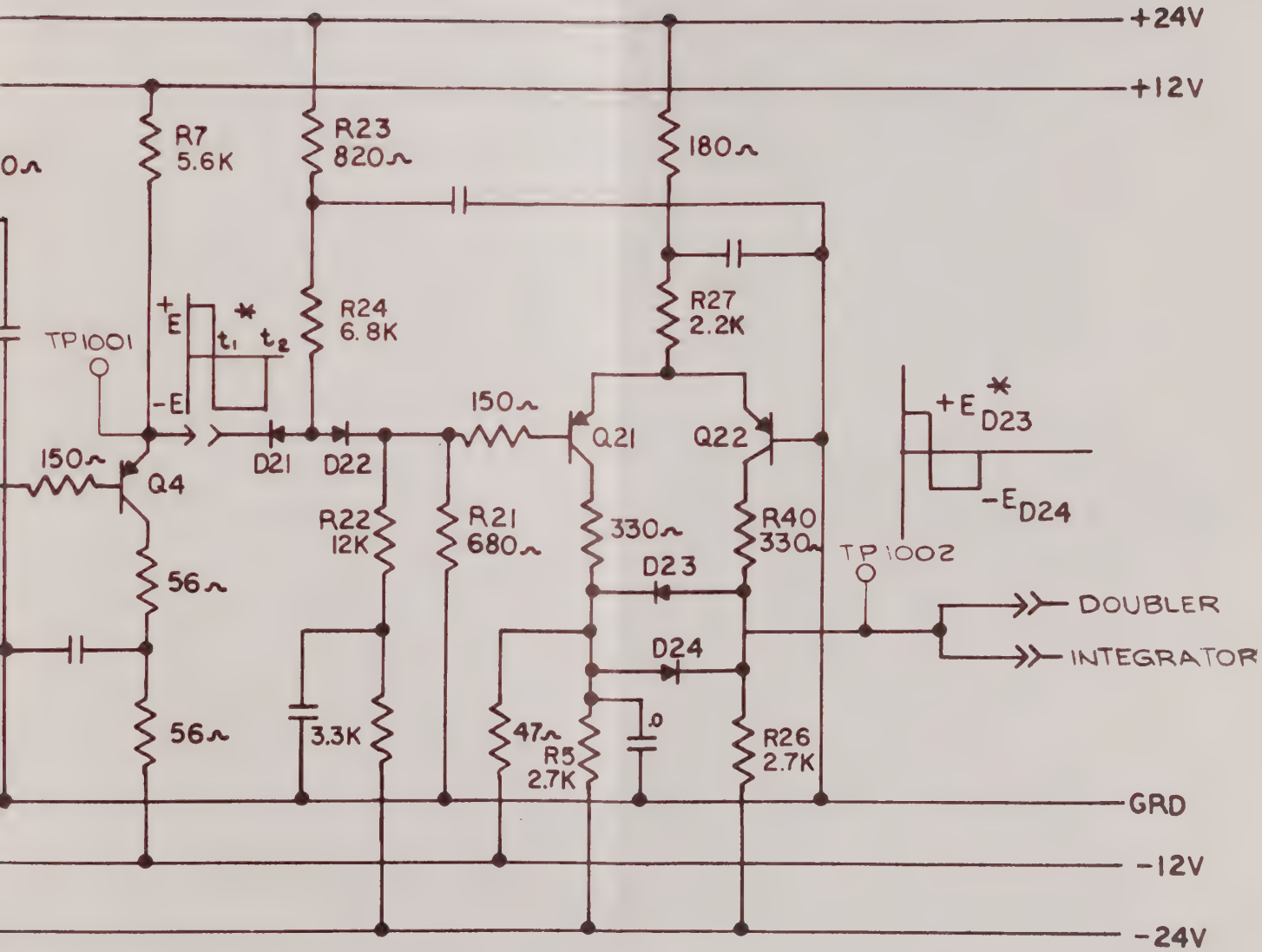


Figure 4-4. DC Restorer Circuit

a. A phase locked loop consisting of the doubler, phase comparator, loop filter, DC amplifier, and voltage controlled oscillator, is used to generate an internal timing signal by locking onto the input data frequency.

b. A new data signal is generated by integrating the input signal at times governed by the timing signals generated in the phase lock loop, and then detecting the integrated wave to establish the reconstructed output data.

The phase lock loop is a method of generating a timing signal (called VCO) from the noisy jittering input data. A voltage controlled oscillator, the center frequency of which is the nominal bit rate of the input data, is jittered at the same rate and phase as the input data through a phase locking feedback loop. Since data is always relative to clock in the format synchronizer sections, this is equivalent to eliminating jitter from the data. The timing signal, VCO, is used to derive the PCM system clock. For NRZ-L, -M and -S input data codes, the VCO signal becomes the system clock. However, for RZ and Bi-Phase inputs the VCO signal is equal to two clocks; thus, it is divided by two in the format synchronizer section.

The voltage controlled oscillator runs at a nominal rate determined by the tuning unit installed in the bit synchronizer and a VCO quadrature signal is compared with the output signal of the doubler in the phase comparator. Since the doubler output frequency is derived from data, any change in the data frequency with respect to the frequency of the voltage controlled oscillator will produce a voltage in the phase comparator. This voltage, when fedback to the VCO through the loop filter and DC amplifier will pull the VCO frequency back in correspondence with the data. When this correlation is maintained,

the phase lock loop is "locked", the locked voltage controlled oscillator generates the VCO (and $\overline{VCO}$) signals which control integration and bit detection.

The input data is also applied to the integrator where a "1" or "0" decision is made based on the average power in given time increments. Since the integrator is tuned by the VCO signal, integrations are performed at the exact incoming data bit rate. The positive ("1") or negative ("0") integrations operate a current switch and flip-flop in the bit detector which generates a new serial data train.

4.4.1 DC Restorer and Limiter

The DC Restorer eliminates gallop by shifting the DC level of a signal to produce an output with symmetrical positive and negative peaks. Figure 4-4 is a simplified schematic of the DC Restorer.

Assume prior to t = 0 an input signal has charged capacitors C1 and C2 to the magnitude and polarities shown. The charging signal may differ from the indicated signal in waveform but not appreciably in positive and negative magnitudes. Because of the long discharge time constant, the C1 and C2 voltages will be only slightly less than those indicated.

The input to the DC Restorer circuit consists of the R0, D1, D2 limiter circuit and two buffer amplifier stages. If the input signal exceeds plus or minus 12 volts, diode D1 or D2 is forward biased and will limit the Q1 base at the corresponding supply potential. Q1 and Q2 are in a unity gain emitter-follower configuration, hence, the Q1 input signal appears across resistor R1.

When the signal becomes positive at t = 0, diode D4 is forward biased and transistor Q2 charges C2 to the value indicated. Because D3 is reversed biased, the Q3 base signal is equal to the input signal (3E/2) plus the C1 voltage (E/2) minus the voltage drop across R5. Similarly, when the signal becomes negative, D3 is forward biased and D4 is reversed biased; and the net Q3 signal is the input signal (-E/2) plug the C2 voltage (-3E/2), plus the voltage across R6. In either case, the voltages across R5 and R6 are equal in magnitude (assumed here to be exactly E), and the Q3 base signal is symmetrical about DC zero level.

Transistors Q3 and Q4 are unity gain emitter-follower amplifiers, the zero centered amplitude symmetrical Q3 base signal appears at the output of the DC Restorer.

Although capacitor C3 is not necessary to the DC restoring operation it is necessary to preserve proper data bit waveform. Capacitor C3 bypasses the clamping circuit to prevent RC (circuit resistance - Q3 junction capacitance) attenuation of the high frequency signal components.

When the output of the DC Restorer circuit is zero, the total current flowing through R24 places the junction of D21 and D22 at zero volts. Any positive input signal, reverse biases there diodes, and a positive voltage will be developed across R21. Similarly, a negative input signal forward biasing D21, and the negative supply reverse biasing D22 develops a negative voltage across R21.

The positive voltage across R21 reduces the Q21 emitter-base current, and the total Q21 current component in R27. Since the base potential of Q22 is fixed at zero, the Q22 emitter-base drive is increased to maintain the total current in R27 constant. The increased Q22 collector current develops sufficient voltage across R26 to forward bias D23 through R27 to the minus 12 volt supply. The forward biased D23 now carries the additional Q22 current and maintains the limiter output at -12 V plus the voltage drop across D23.

Similarly, a negative signal across R21 increases the forward current in Q21 and therefore reduces the Q22 current in R26. Diode D24 is now forward biased on the -12 volt supply and the output voltage is -12V minus the voltage drop across D24.

4.4.2 Phase Comparator

The Phase Comparator, illustrated in Figure 4-5, compares two 180° out-of-phase quadrature VCO signals with the DATA doubler outputs. When these two signal pairs are in phase (same frequency) the average output of the Phase Comparator is zero. The Phase Comparator consists of two AND gates D1 - D2 and D3 - D4, and OR Gate D5 - D6. The junction of D5 - D6 is at 0 volts whenever both AND gates are open. When either AND gate closes, D5 or D6 is reversed-biased so that its common junction goes positive or negative. When 2XDATA and QUAD VCO are both negative, D5 is reversed biased due to AND gate D1 - D2 closing, and a negative voltage appears at the output junction. When QUAD VCO and 2XDATA are both positive, D6 is reversed-biased to produce a positive voltage at this junction. The resultant uniform output waveshape averages to zero in the loop filter. When the two input signal pairs change phase by slipping

with respect to each other, the output waveshape becomes non-uniform with net positive or negative pulses, depending upon the direction of the phase change. These non-uniform pulses are averaged in the loop filter to produce voltages which control integration, bit detection, and correct the VCO frequency in a direction to cancel the original phase difference.

4.4.3 DC Amplifier

Under steady state conditions, the loop filter output voltage is zero and the frequency adjust potentiometer R10 controls the frequency of the VCO. The setting of R10 determines the Q5 base current which in turn determines the Q5 collector current through R8. Since Q4 is always forward biased, the resulting constant voltage developed across R8 forces Q4 to appear as a constant voltage in series with R6 and Q3 to set the potential level of the frequency control bus (FCB). Filter capacitor C3 in parallel with Q4 smooths any voltage variations tending to appear across Q4.

If the loop filter voltage rises, the resulting increase in voltage across R2 reduces the current through the forward biased temperature compensating diode, D1. As the D1 component of current through R3 decreases, a current component will flow through R3 and R4 to increase current in R11.

As the R11 voltage increases, the Q3 base potential is lowered sufficiently to permit an increase in base drive signal. The resulting increase in Q3 collector current divides between R8 and the Q4 base circuit and the collector-emitter junction of Q4. The Q4 emitter current flowing through R6 in effect compensates for the decrease in Q3 voltage to (1) increase the potential of the frequency control bus, and (2) develop the output signal to the phase comparator.

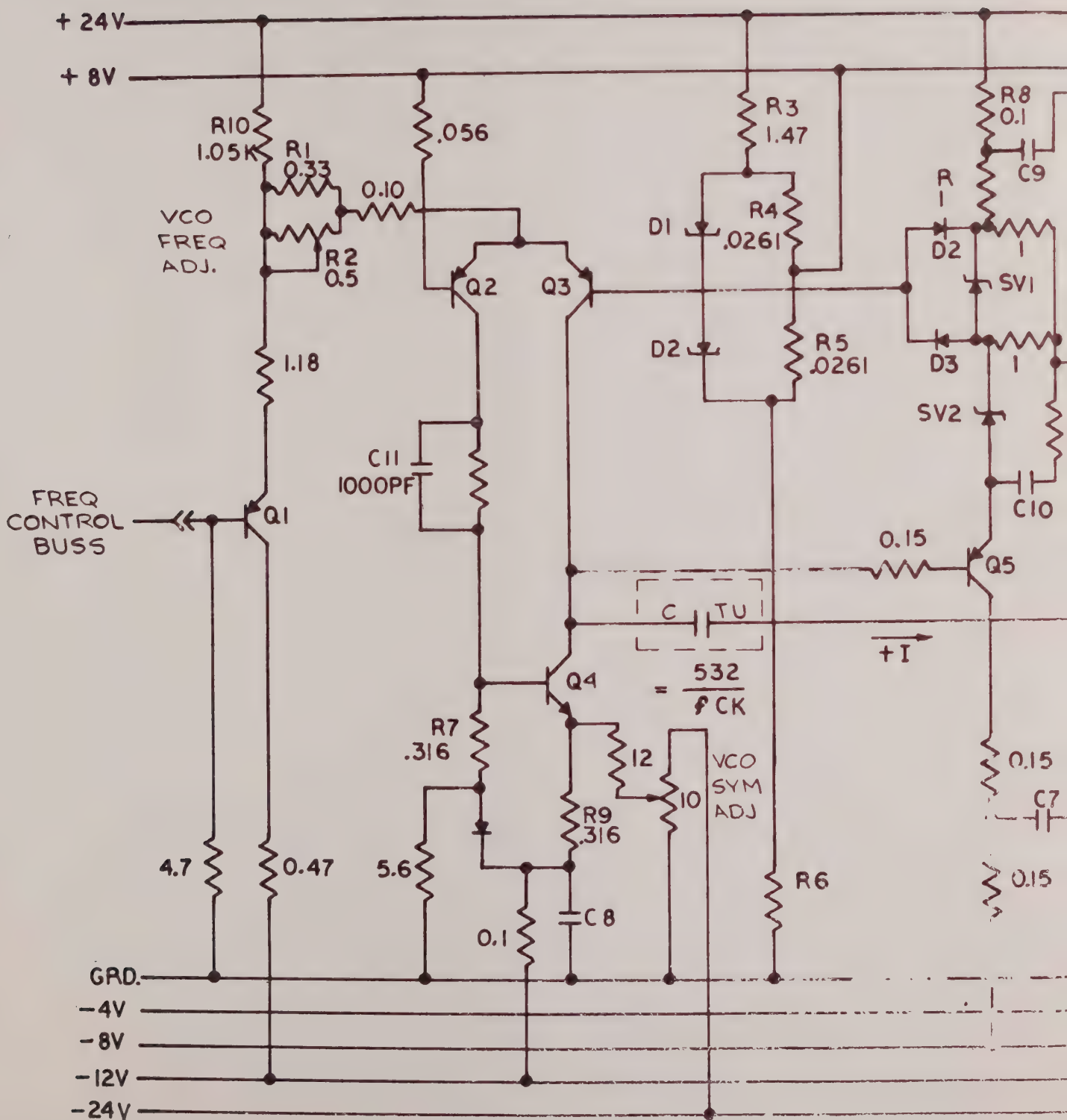
4.4.4 Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) generates the VCO and $\overline{VCO}$ signals synchronous with the input data. The Quadrature Amplifier develops from a VCO signal a comparable signal displaced in time by 1/4 period from the true VCO signal (See Figure 4-6).

Assume that the Frequency Control Bus (FCB) signal is zero and only the DC currents are flowing in the Q1 input circuit. Under these conditions the VCO is operating as a free-running square wave oscillator at a frequency determined by the capacity C_{tu} Resistors R3, R6 determine the voltage of the series tunnel diodes (TD1 + TD2) such that when one tunnel diode is "ON" the other is "OFF". For the balance of this discussion, assume that TD2 is switched ON.

With TD2 OFF, Q3 is biased on. Since the Q2 base is held at a constant potential, the emitter circuit voltage decrease due to the Q3 current, is sufficient to bias Q2 OFF. When the voltage across R7 drops to zero, the forward-biased diode, D1, places Q4 close to cut off to permit the charging of C_{tu} by the Q3 current.

The increasing voltage developed across C_{tu} reduces Q5 emitter current through R8. As the voltage across R8 decreases, the forward voltage across diode D3 increases until D3 passes current through TD2. When the increasing capacitor voltage reaches a value such that the total tunnel diode current attempts to exceed the peak value; TD2 switches the ON state and TD1 switches to the OFF state. With TD2 ON, Q3 is reversed biased to cut off and Q2 is again forward-biased to conduction.


+ 24V
+ 8V
R10
1.05K
R1
0.33
0.10
.056
VCO
FREQ
ADJ.
R2
0.5
1.18
Q2
Q3
R3
1.47
D1
R4
.0261
D2
R5
.0261
R8
0.1
C9
R
1
D2
1
SV1
D3
1
SV2
C10
C11
1000PF
FREQ
CONTROL
BUSS
Q1
0.15
Q5
C
TU
+I
Q4
= 532 / f CK
R7
.316
12
10
VCO
SYM
ADJ
R9
.316
0.15
C7
4.7
0.47
5.6
C8
0.1
R6
0.15
GRD.
-4V
-8V
-12V
-24V

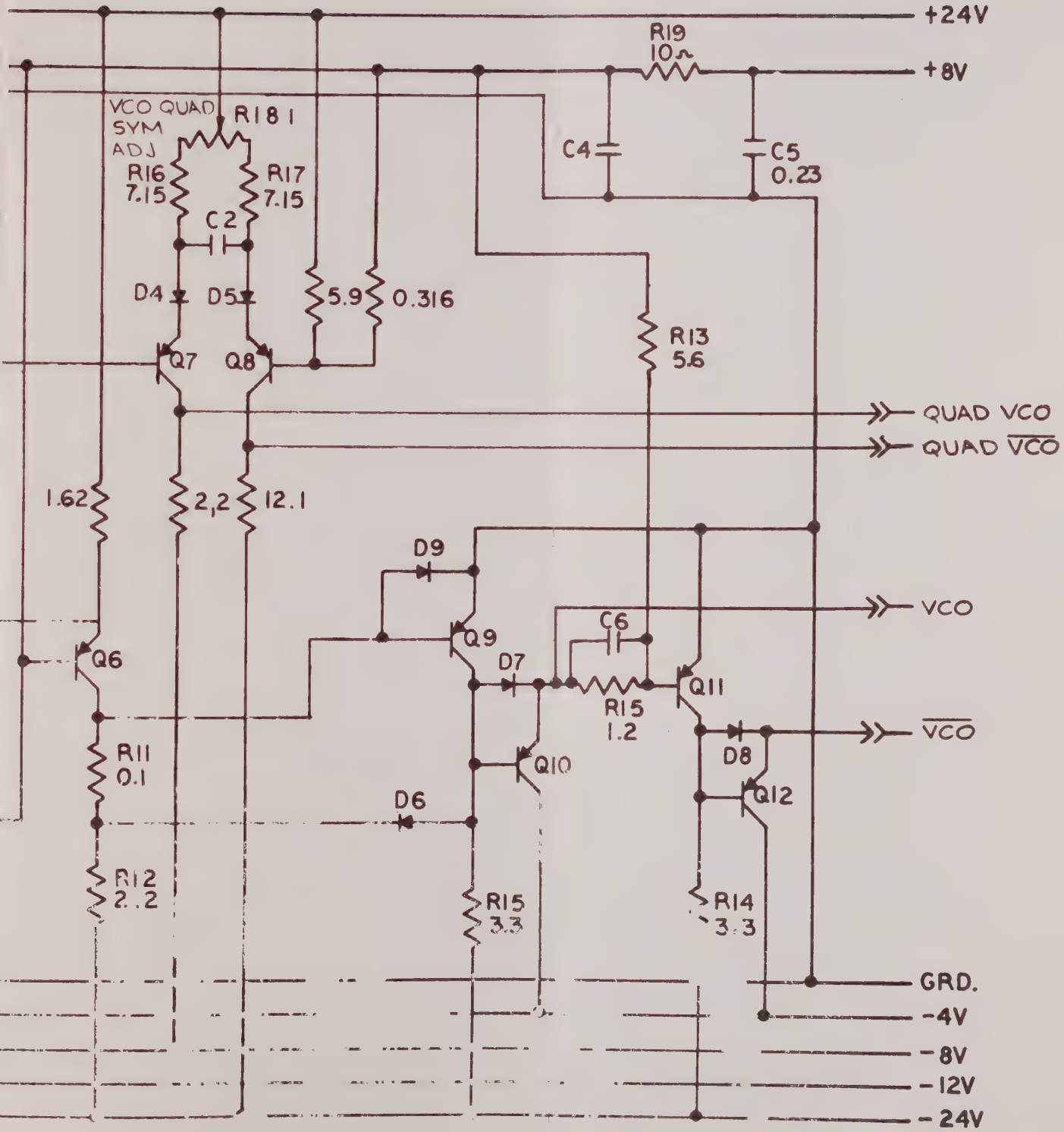


Figure 4-6. VCO and Quadrature Amplifier Circuit

When Q2 conducts, a portion of the collector current serves to forward bias Q4, which discharges capacitor C_{tu} through Q4. Because of the nearly identical parallel networks R7 - D1 R9, and the Q4 base-emitter junction diode) equal currents flow in(R7 and R9. As Q2 collector current is constant, Q4 discharges C_{tu} at a constant rate. (Potentiometer R30 provides a fine adjustment to equalize the charging and discharging rates).

In a similar manner, the decreasing voltage across capacitor C_{tu} forward biases Q5 which causes TD1 to conduct, and TD2 to cut-off.

Frequency control is achieved by varying the charging rate of capacitor C_{tu}. If the input signal decreases to forward bias Q1, the increasing voltage across R10 will lower the Q2 and Q3 emitter potentials, decreasing the collector currents. Since the collector currents determine the charging rate, and therefore the frequency; the frequency is lowered accordingly.

The VCO signal is derived from the isolation transistor Q6 which is a unity current gain common base amplifier. Consequently the current through the associated capacitor is transferred as a voltage square wave across resistors R11 and R12.

When the Q9 base potential increases positively, the current through Q9 decreases to lower the Q9 collector potential. Diode D7 is reverse biased and R15 current flows from Q10 base, driving Q10 to saturation at -4 volts which produces a negative VCO output.

Increasing voltage across R15 causes Q11 collector current to increase driving Q11 to saturation and forward biasing D8.

A negative input signal to Q9 interchanges the roles of the two transistor stages. Transistor stages Q9 and Q10 and Q11-Q12 then operate as described in paragraphs above.

Diode D9 affords Q9 emitter-base junction protection for excessive reverse bias by clipping the positive Q9 base signal peaks; diode D6 clips the negative signal peaks.

The Quadrature Amplifier derives its input signal from the integral of the current square wave passing through an associated capacitor. The axis crossings of the resulting triangular voltage wave are sensed by the Q7-Q8 current switching circuit to produce a voltage square wave displaced 90° from the current square wave.

The triangular voltage wave is applied to the base of Q7. Currents flowing through resistors R16, and R17 are switched alternately into Q7 and Q8 emitters. If the input wave is above its centerline, the current is switched to Q7, and through Q8 if the input wave is below its centerline. Transistors Q7 and Q8 act as common-base current transfer elements; that is, the emitter current appears as a collector current which then flows through the collector load resistors to produce the output voltage. These transistors never saturate.

To understand the operation of this circuit, consider C2 to appear as a low impedance path for the AC components of the triangular wave. When the input wave goes below its centerline, the base and emitter of Q7, D4, and C2 all go down with it. This reverse biases D5, causing all R17 current to flow through C2 and Q7 for one half cycle. When the input signal goes more positive than its centerline, D5 and C2 assume the base potential, approximately, of Q8. Diode D4 becomes reversed-biased, forcing R16 current flow through C2, D5 and Q8.

The two Quadrature Amplifier outputs are obtained from the collectors of Q7 and Q8. The Q7 output is the QUAD VCO signal which is compared with the Doubler outputs in the Phase Comparator. The QUAD $\overline{\text{VCO}}$ signal cancels the undersirable high frequency components of the QUAD VCO signal in the Phase Comparator.

4.4.5 Integrator Circuit

This circuit (Figure 4-7) integrates the input signal over a time period controlled by the $\overline{\text{VCO}}$ signal. The integration minimizes the effects of noise on the data signal and develops a uniform Bit Detector control signal with the same polarity as the input signal.

Assume the input signal has been negative for some time before the positive signal at t = 0. With a negative input signal transistor Q1 is cut off, and transistor Q4 is conducting to charge C1 in the negative direction. The +24 volt supply through R3 and R12 forward biases diodes D1 and D3 to the +12 volt supply, therefore, the Q3 emitter-base potential is zero and Q3 is cutoff. Initially, neglect the effect of Q2.

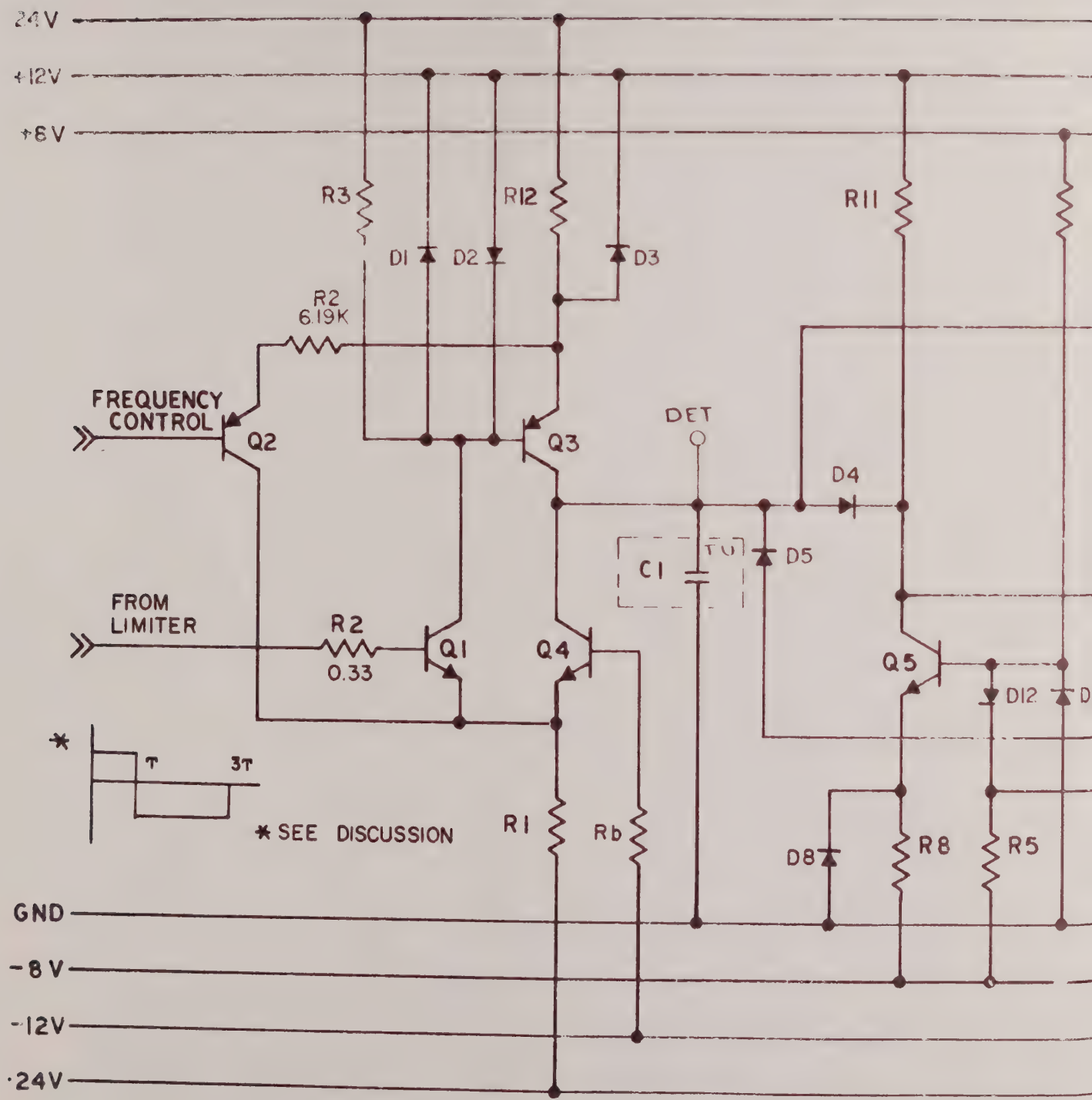
The Q1 component of current in R12 now forward biases Q3 to conduction and Q3 begins to charge C1 in the positive direction. At the same time, the Q1 component of current in R1 increases the Q4 emitter potential sufficiently to cut-off Q4. Because the Q1 current also flows in R3, the Q3 base potential decreases with the decrease in emitter potential until diode D2 conducts to carry the remaining Q1 current.

Transistor Q3 continues to charge C1 until the input becomes negative at some later time. A capacitor is again discharged to permit Q4 to charge C1 to the same negative polarity as the input signal.

At time T, the negative input signal reverse biases Q1 to cut off. The Q1 current components in R3 and R12 are now zero and Q3 is cut off (note paragraph above). The Q4 base-emitter current increases to compensate for the loss in Q1 emitter current and Q4 conducts to charge C1 in the negative direction.

AT 2T the discharge circuit reduces the C1 voltage to zero. Because the input conditions have not changed, Q4 continues to charge C1 in the negative direction.

Before considering the operation of the C1 discharge circuit, note that transistors Q5 and Q6 are normally in the cut off or open circuit condition; transistor Q5, because the emitter-base potential is held to zero by the forward biased diode, D8 (-R8), and D11, D12 (-R5); and transistor Q6, because of the forward-biased diode D6 (-R6) and D9, D10 (biased) through R11, R7. Because Q5 and Q6 are cut-off, the circuit voltages are such that diodes D4 and D5 are reversed biased and represent open circuits to the C1 plus and minus voltages. Note also that the Q6 input circuit is responsive only to negative input signals, positive signals being shorted to ground through diode D10. At time T, the C5 differentiating capacitor converts the negative going $\overline{VCO}$ signal to a current spike to momentarily turn on Q6. When Q6 conducts, the voltage spike developed across R4 also appears (through C2) across R5 to turn on Q5. As Q5 conducts, its collector potential decreases to further drive Q6 into conduction through the positive feedback path of R7 and C7. The net result of the intercoupling between Q5 and Q6 is an extremely rapid turn-on of both transistors.


24V
+12V
+8V
R3
R12
R11
D1
D2
D3
R2
6.19K
FREQUENCY
CONTROL
Q2
Q3
DET
D4
C1
D5
FROM
LIMITER
R2
0.33
Q1
Q4
Q5
D12
T
3T
* SEE DISCUSSION
R1
Rb
D8
R8
R5
GND
-8V
-12V
-24V

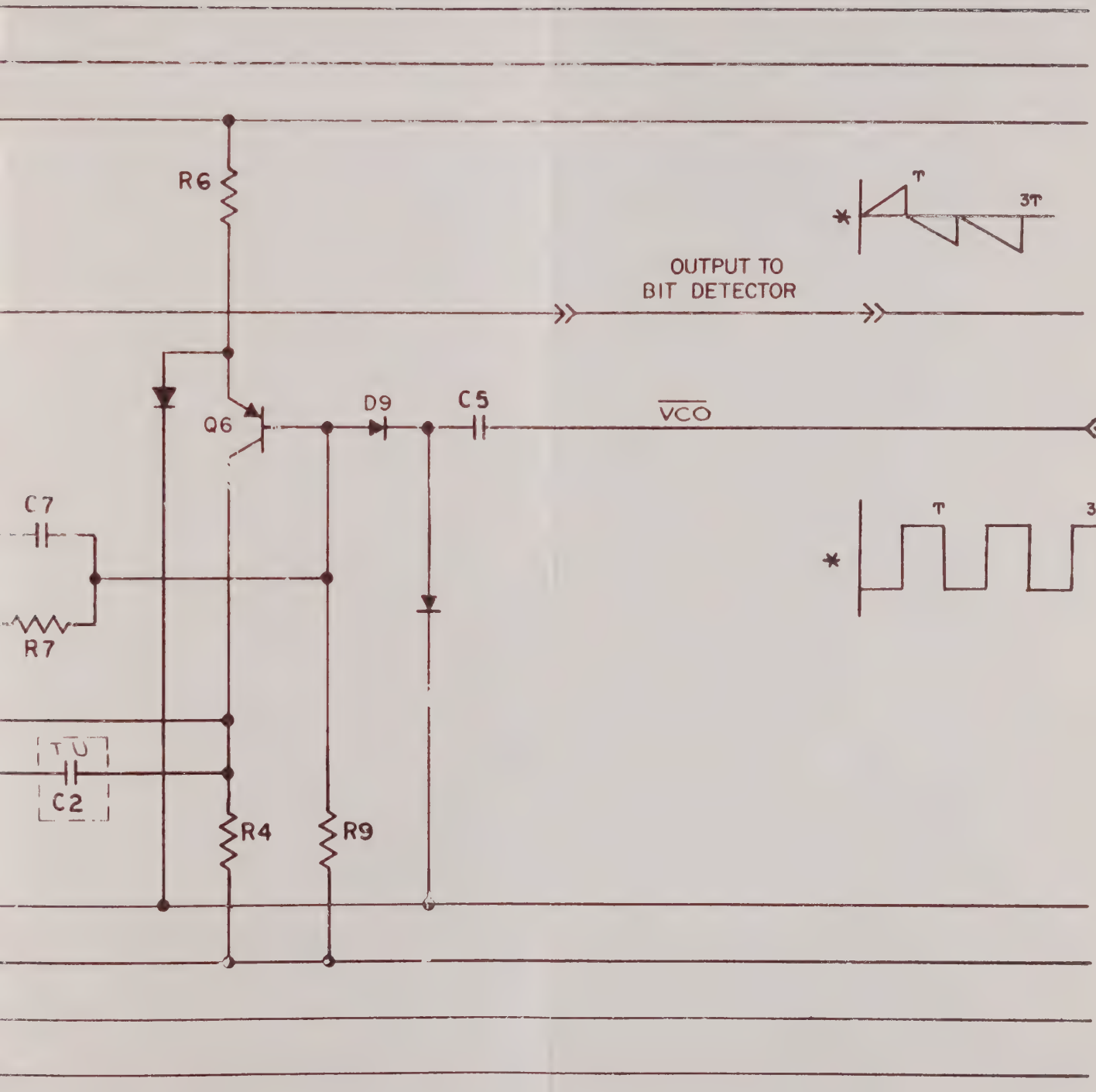


Figure 4-7. Integrator Circuit

When transistors Q5 and Q6 are fully ON, diodes D4 and D5 are forward biased to discharge C1 by placing the ungrounded C1 terminal at ground potential. Whereas the complete C1 discharge path is awkward to visualize, Q5 may be considered to discharge C1 to zero voltage and Q6 to charge C1 to zero voltage. (The following voltage equations indicate the conditions for zero C1 voltage: EC1 = EQ5 - (ED8 - ED4), EC1 0 and -ED1 = EQ6 - (ED6 - ED5), ED1 0 where EC1 is considered a source and the remaining polarities are determined by the direction of positive current flow).

The circuit time constants are such that Q5 and Q6 remain ON until C1 is fully discharged. When the voltage across C1 is essentially zero, Q5 and Q6 return to the OFF conditions until again triggered ON by the trailing edge of the next $\overline{VCO}$ pulse.

Transistor Q2 with input from the frequency control bus (FCB) provides a shunting path around Q3 and Q4 to ensure a constant C1 output voltage level. If a DATA frequency shift occurs to reduce the data bit period, C1 would tend to charge to a lower output voltage level. In this event, the FCB signal would increase the charging current of either Q3 or Q4 to develop a normal C1 output voltage.

4.4.6 Bit Detector Circuit

The Bit Detector Circuit (Figure 4-8) generates a new DATA signal in time phase with the VCO signal. The signal has a fast rise time and is free from the noise and distortion of the original DATA signal.

Assume initially that the VCO pulse at t = 0 has switched transistors Q4 and Q6 ON and transistors Q5, Q7, and Q8 OFF. For convenience, the quiescent current through Q1 will be assumed to divide equally between Q2 and Q3.

As the positive signal increases to reverse bias Q2, the Q2 current decreases and the Q3 current increases to the full quiescent value. Because of the current limiting of Q1, Q3 can pass this current, but the voltage developed across R3 is too small to trigger the heavily biased Q5.

Because of the short time constant of the Q1 input circuit, only the leading edge of the positive going clock pulses appear in the Q1 circuit. Negative pulses are short circuited to the +8 volt supply by diode D1 and diode D2 is reversed biased to the small voltage appearing across D1.

At the end of the VCO signal period T, the leading edge of the positive VCO pulse momentarily increase the forward drive to Q1 which starts to conduct. As Q2 is reversed-biased by the input signal, the current spike passes through Q3 to develop a voltage across R3 sufficient to forward bias Q5. The resulting Q5 current in R7 lowers the Q5 collector potential to reduce the forward drive on transistor Q8 and therefore the voltage across R12. The reduction in R12 voltage felt across the R10 - R4 voltage divider, reverse biases Q4 cutting it off. The Q4 component of current in R6 is now decreasing, and the increase in Q4 collector potential forward-biases Q6 to conduction. Note that the DATA and $\overline{\text{DATA}}$ circuits each provide positive feedback paths to increase the speed of the Q4, Q5 current switching circuit. The net result is an output signal waveform with minimum rise and fall times.

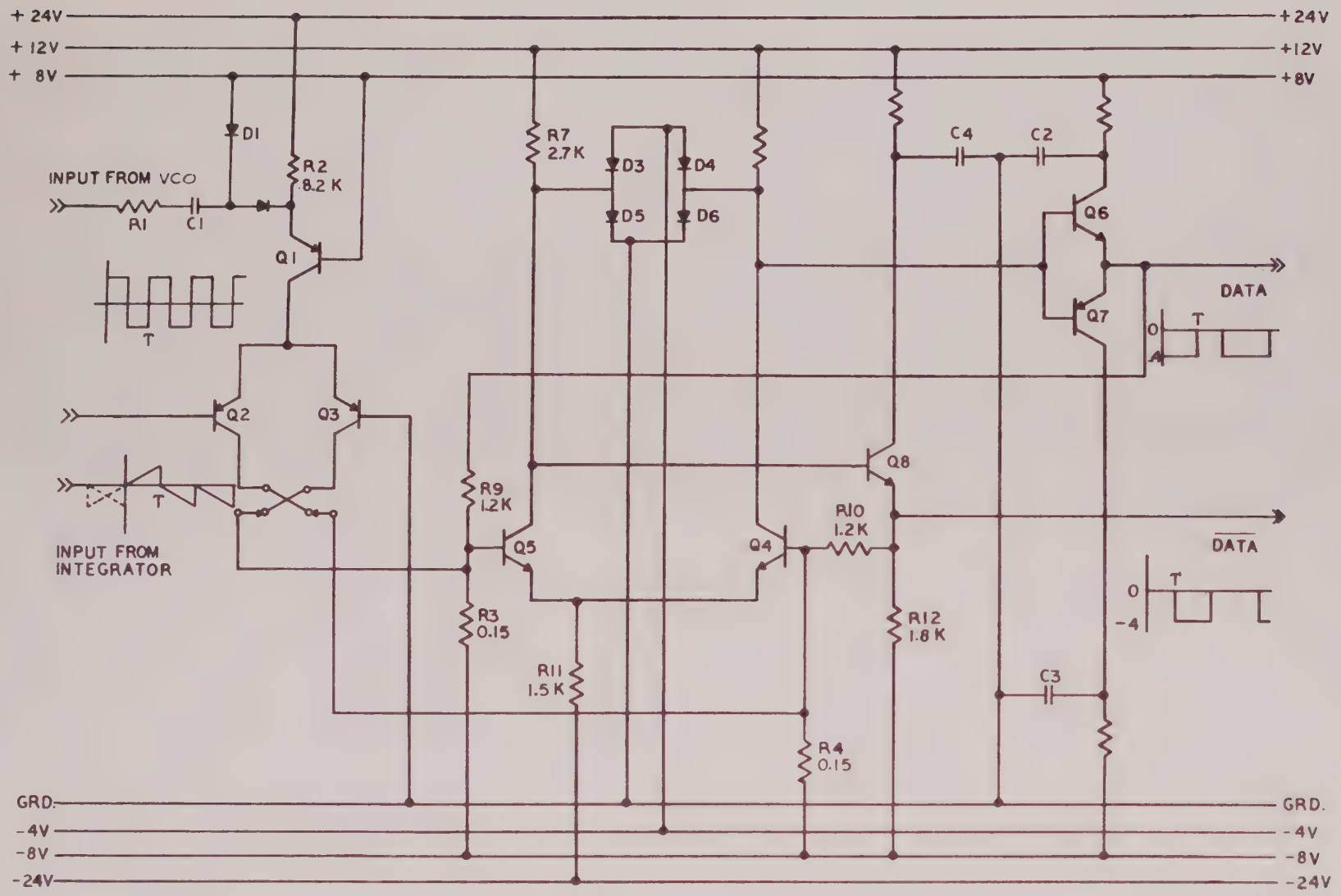


Figure 4-8. Bit Detector Circuit

As Q5 approaches full conduction, the voltage across R7 increases until diode D3 is forward biased to hold the Q5 collector at -4 volts. Similarly, as Q4 approaches cut off, the voltage acorss R6 decreases until D6 is forward biased to hold the Q4 collector at 0 VDC.

As the emitter potentials of the emitter-follower (Q8), or the complementary emitter-follower (Q6) and (Q7) approach those of the forward biased base, the DATA and $\overline{\text{DATA}}$ signals are -4 and 0 volts, respectively.

In the interval T - 2T, the forward bias on Q2 is increasing and shifting the quiescent current from Q3 to Q2. Because Q4 and Q5 are heavily biased by the positive feedback paths the output conditions remain constant during this interval.

At time 2T the positive leading edge of the VCO pulse again triggers Q1. As Q2 is now forward biased by the input signal, a comparable sequence of events occur resulting in Q4 and Q7 turn-on, and Q5 and Q8 turn-off and the indicated output levels.

A polarity reversing switch is incorporated in the Bit Detector circuit in the event that the system requirements dictate an inverted DATA output signal. Operation of the switch interchanges the roles of Q4 and Q5; thus reversing the DATA and $\overline{\text{DATA}}$ output signals.

4.4.7 Meter Circuit

The metering circuit (Figure 4-9) compares the VCO frequency with the data signal to generate a meter signal roughly proportional to the bit error loss. In the presence of severe noise or data, or signal fading sufficient to disrupt the phase-lock-loop, the metering circuit produces a positive indication of loss of phase lock.

The triangular VCO signal is clipped on top and bottom by diodes CR1 and CR2, and amplified by the Q3401 inverter. Q3402 and Q3403 are connected as a Schmitt Trigger to square up the clipped and amplified VCO signal which now appears as a square wave at the Q3403 collector. The frequency of this square wave is the original VCO signal frequency. The squared VCO signal is inverted once by Q3404, and inverted again by Q3405 to provide two identical signals 180 out of phase with each other. The Q3404 and Q3405 outputs are the SET and RESET signals respectively, for the flip-flop consisting of Q3406 and Q3407. DATA taken from the Doubler output of the SBS-2 is inverted by Q3408 and applied to the SET gate and RESET gate of the flip-flop.

When the SBS-2 is in lock, the VCO signal and DATA corresponds to phase and frequency so that the fixed relationship of SET, RESET and SET gate, and RESET gate cannot make the flip-flop change state. As a result C12 remains charged to the DC voltage obtained at the Q3407 collector and no current flows in the meter or diode bridge. As the DATA rate begins to "slip" with respect to the VCO rate, Q6 and Q7 begin to change state since their set and reset inputs (VCO) no longer have fixed phase relationship with the set and reset gates (DATA). Consequently, the flip-flop changes state at a rate proportional to the difference in VCO and DATA rate. Capacitor C12 charges and discharges according to the voltage change at the Q7 collector, and the resulting current is rectified by the diode bridge to deflect the meter. Since the meter detects average current, its deflection will be proportional to the severity of loss-of-lock in the SBS-2 phase-lock loop. Full meter deflection indicates complete loss of lock. At small differences of VCO and DATA rates the meter deflection will oscillate due to the slow charge and discharge of C12. As the frequency

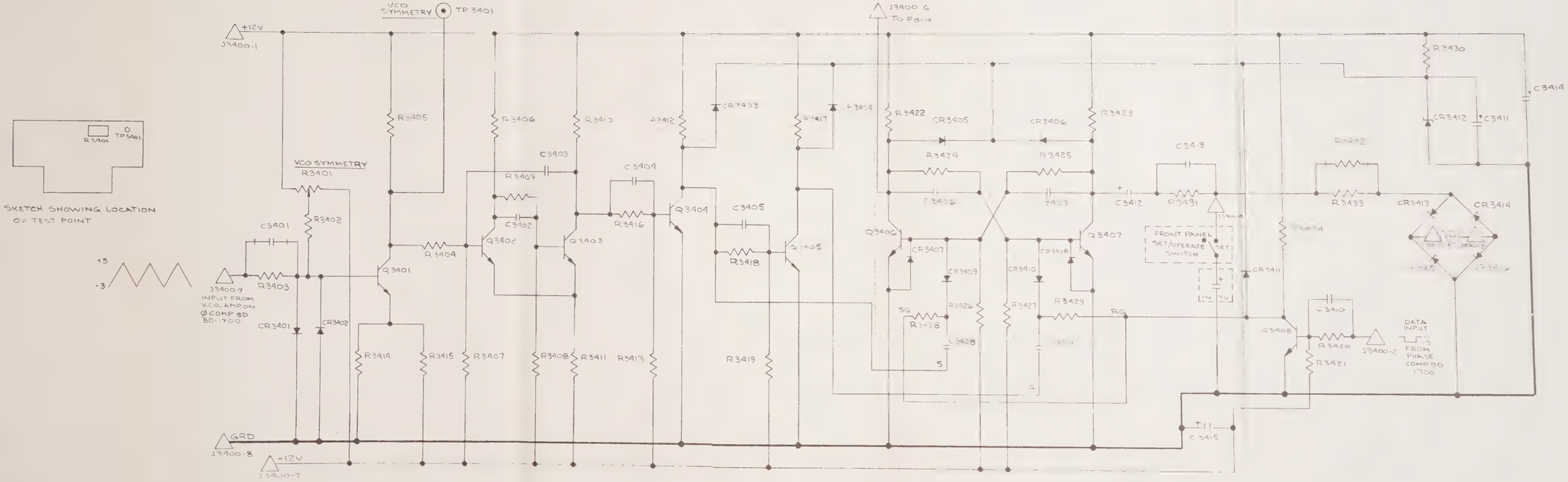


Figure 4-9. Meter Circuit

difference becomes greater, the meter deflection tends to stabilize at the average current magnitude. Either noise or out-of-lock conditions may cause a meter deflection.

To adjust the tuning unit to the VCO center frequency, the Phase-Lock Loop is opened when the mode switch is in the SET position. In the SET position, a capacitor located in the tuning unit is a low pass filter for the Q3407 output. At the VCO center frequency, the Q3407 output causes full meter deflection because of the low pass capacitor. As the VCO approaches its center frequency, the meter approaches full scale. Detuning the VCO results in meter oscillations representing the frequency difference from the center frequency.

4.4.8 DC Power Sources

The SBS-2 requires external power supply voltages of +24 volts and -24 volts. These input voltages are used directly on the various plug-in modules and also in conjunction with two self contained power supply modules to generate the secondary DC voltages required for operation of the SBS-2. The secondary voltages consist of -4 volts ±8 volts and ±12 volts. The power supplies are standard series regulators to produce minimum output impedance at the voltage levels determined primarily by the input voltage divider circuits. Schematics of both positive and negative power supply modules are contained in Section V.

4.5 FORMAT SYNCHRONIZER

In the following paragraphs, each circuit of the Format Synchronizer section is discussed. Figure 5-4 illustrates the location of each circuit, and the role the assembly plays in the decommutation process may be derived from Figure 4-2.

4.5.1 Data Input and Control Logic Assembly 075060

The outputs of the SBS-2 Bit Synchronizer, consisting of data and a synchronous timing signal (VCO) are applied to the data input and control logic assembly 075060. This assembly located in slot 8 of the card file provides the logic to perform various gating and control functions necessary for the operation of the system. These functions are:

a. The couple inputs to the code converter from the SBS-2 Bit Synchronizer.

b. The timing and control of the format counters (word and frame advance and recycling signals in the synchronizer section (synchronizer format counter control logic.)

The logic diagram for the data input and control logic assembly may be found on drawing 075060 in Section VIII. The inputs to the code converter assembly are derived from the outputs of the SBS-2 Bit Synchronizer.

The Synchronizer Format Counter Control Logic contained on this board allows both the word and frame counters to advance one count upon receipt of an ADVANCE pulse from the bit and word counters, respectively, and the resetting of each counter to the correct count

at the appropriate time. The word counter control logic consists mainly of IC 9, 10 and 11. The ADV and APERTURE OR SEARCH lines are high at all times except during a reset operation. Advance (ADV) pulses from the Bit Counter apply signals (ADV WD CTR) to the word counter at the word rate until a sync pattern is detected during the aperture. The RESET WD CTR line is then driven low (IC11-5) resetting the word counter. The clear (CLR) and preset (PST) inputs of the first flip-flop in the word counter are operated separately in order to allow the counter to be reset to a count of 0 or 1 to make the counter programmable.

The control of the frame counter is maintained in a similar manner except that additional control is necessary to accommodate SFID. Flip-flop IC7 is used as a timing adjustment which enables NAND-IC5, and causes the frame counter to advance one count per frame. When the SFID code agrees with the programmed SFID, that is, when proper SFID synchronization is being maintained the UPDATE FR COUNTER (from SFID) line goes high to enable the frame counter to advance at the frame rate. However, if SFID sync is lost so that the pattern does not agree, this line will supply a series of pulses at clock rate advancing the frame counter until its contents agrees with the contents of the SFID counter.

4.5.2 Bit Counter and Code Converter Assembly 070003

The bit counter and code converter assembly is located in card file slot 9 and contains two independent logic circuits, the code converter and the bit counter. A block diagram of this assembly is shown in Figure 4-10.

Data applied to the 4001 PCM System may be NRZ, RZ, or Bi-Phase and the reconstruction of clean data in the bit synchronizer does not alter this input code type. In the bit counter and code converter assembly (070003) all formats are standardized to NRZ-L. However, the input data must be programmed prior to the operation of the system and is accomplished through the use of six spaces on the FORMAT STORAGE CARD. Programming the code converter enables and disables key circuits which convert the general purpose logic of the converter to a simplified equivalent circuit. In addition to code conversion, this converter also accepts the VCO output of the Bit Synchronizer and generates the basic system clock. Figures 4-11 and 4-12, illustrate the equivalent circuits associated with the conversion of each input data type.

a. NRZ-L (Figure 4-12A) illustrates the equivalent circuit derived with an NRZ-L data input and program. In this and all succeeding examples and input data word of 10110001101 has been assumed. Note that no conversion is necessary with this input code and consequently there is no real need for flip-flop IC-6. Refer to drawing 075003 and note that the program lines D and $\overline{D}$ determine which side of flip-flop IC-6 the converter output is derived (a high level on D selects the Q output while a high level on $\overline{D}$ selects

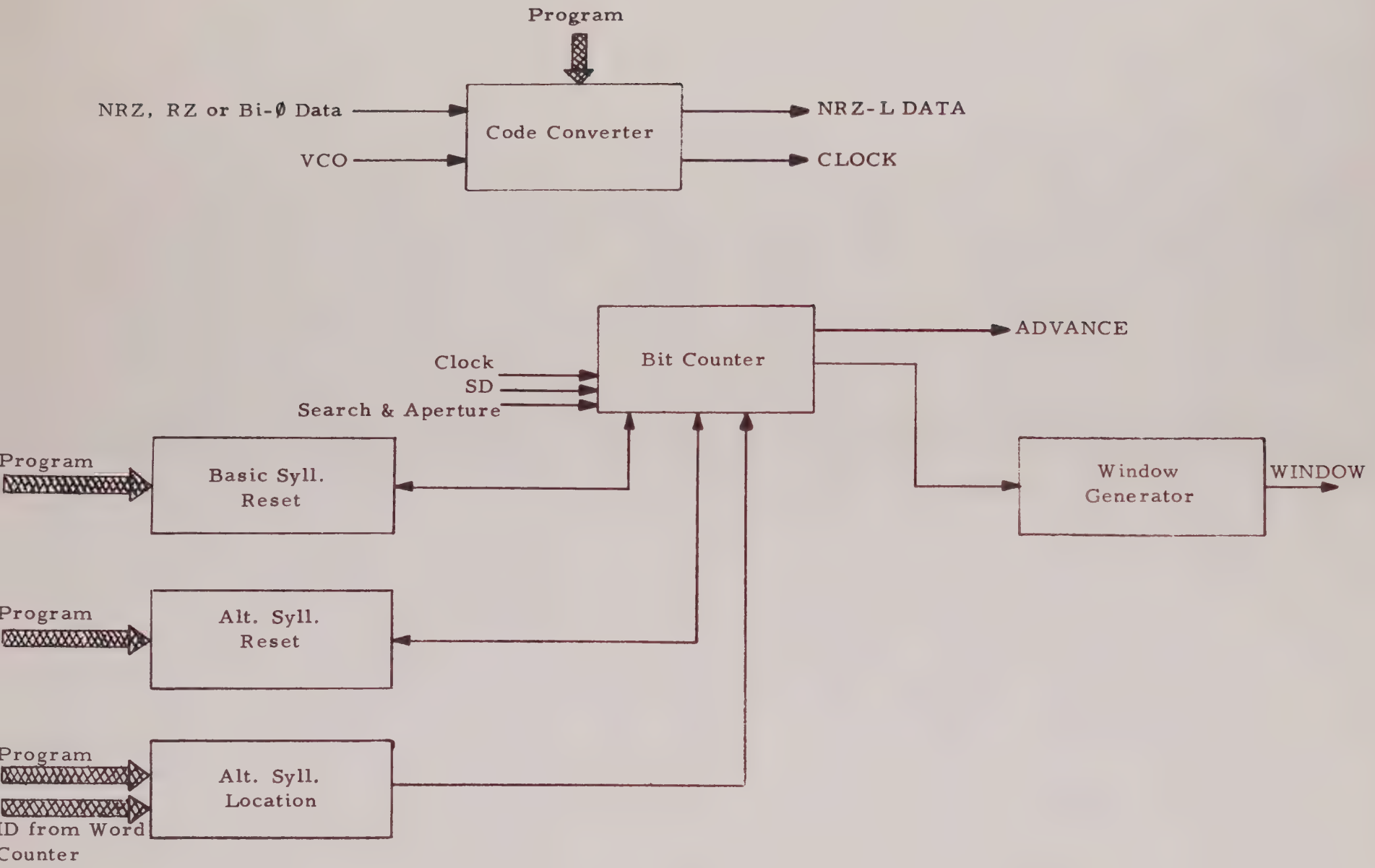
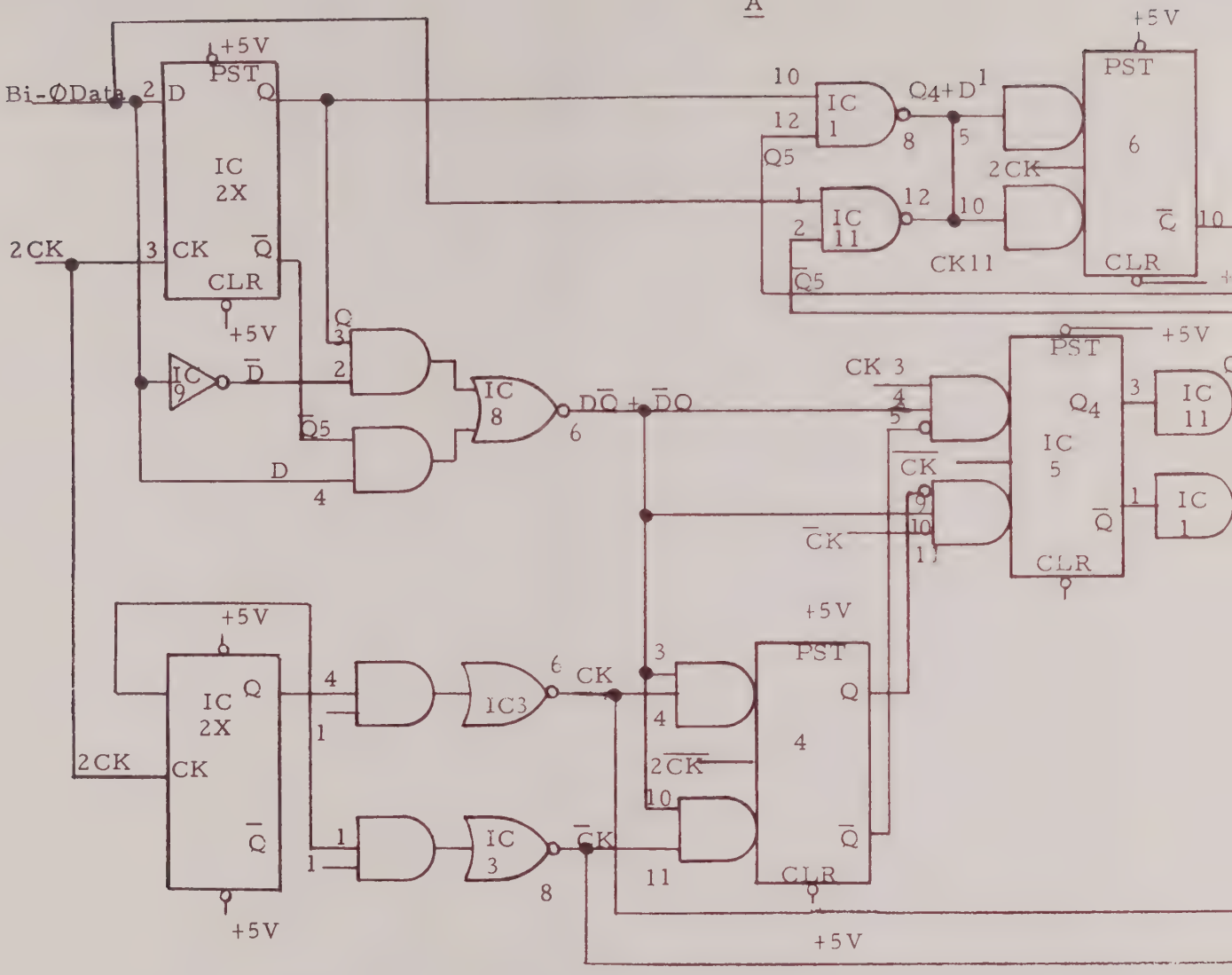
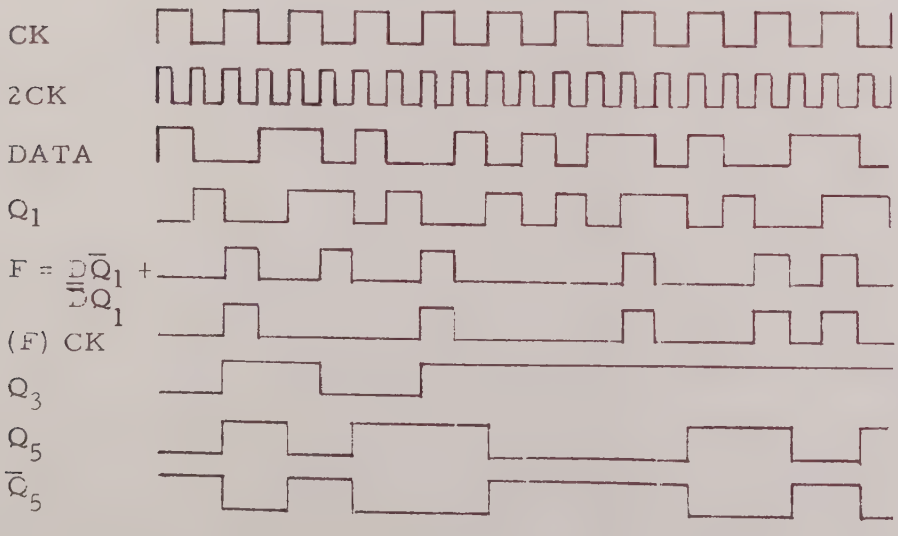
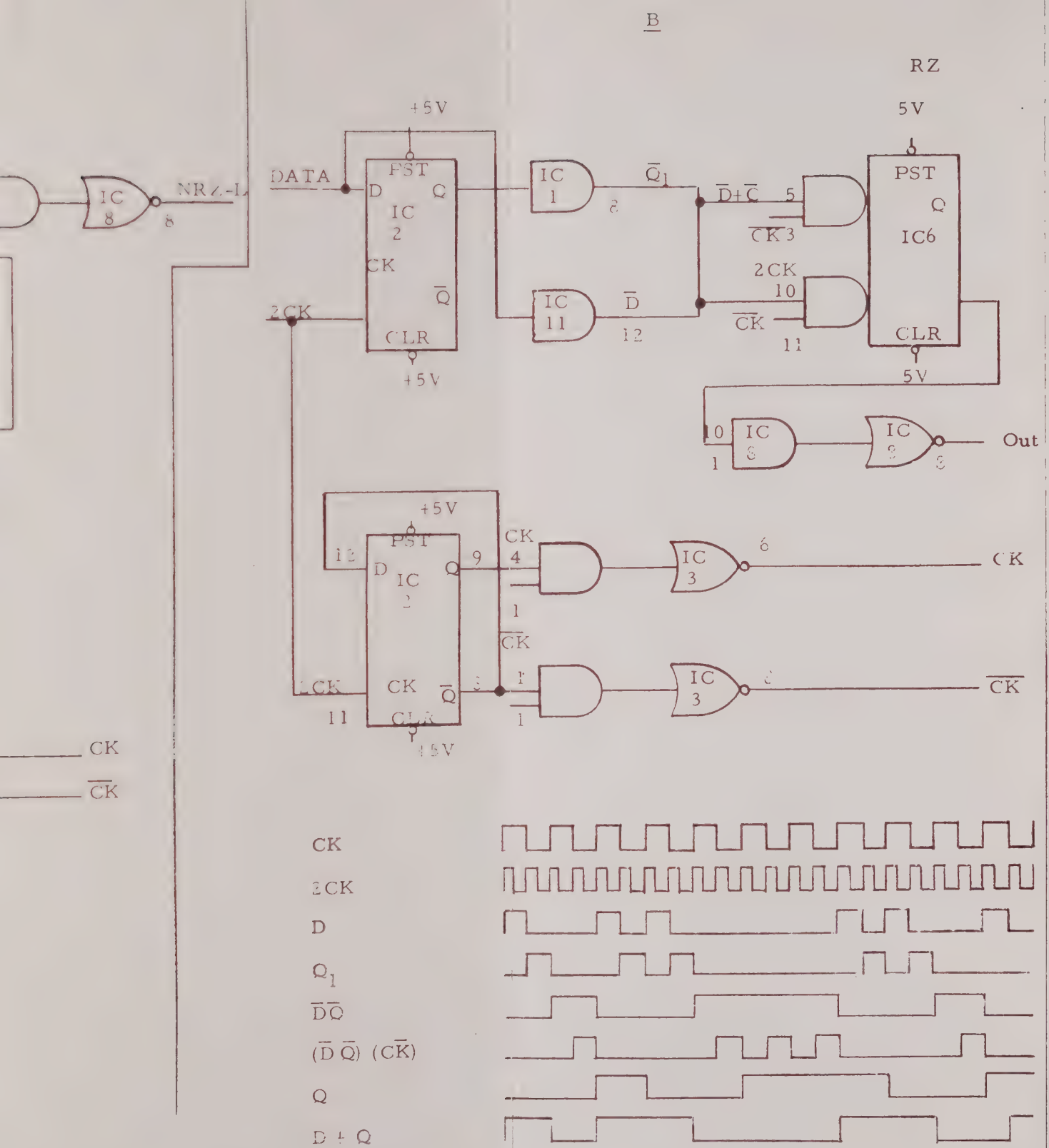


Figure 4-10. Block Diagram, Bit Counter and Code Converter Ass'y. 070003

A


+5V
PST
Bi-ØData
D
Q
IC 2X
2CK
CK
CLR
IC 9
IC 8
IC 1
IC 11
IC 5
IC 4
IC 3
IC 2X
Q4+D
Q5
CK11
DQ̄ + D̄Q
CK
2CK
CLR


CK
2CK
DATA
Q1
F = DQ̄1 + D̄Q1
(F) CK
Q3
Q5
Q̄5

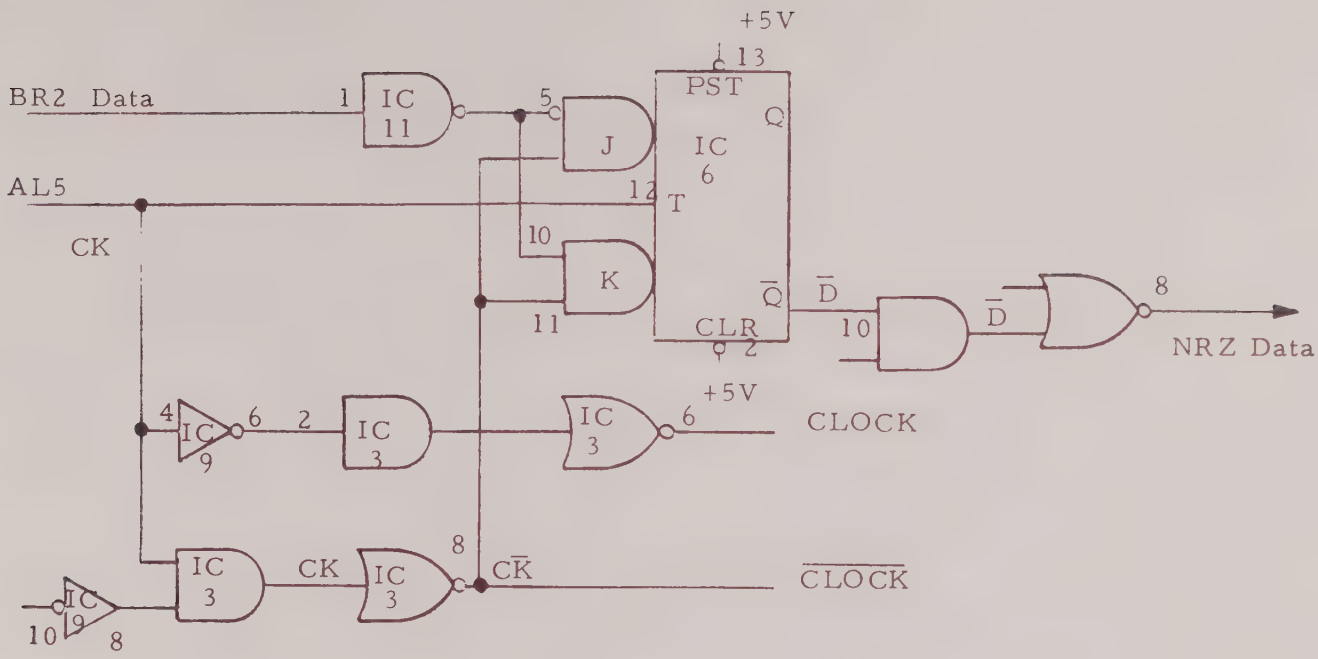


$\overline{RZ}$ utilizes the same circuit except that the Q5 output is used

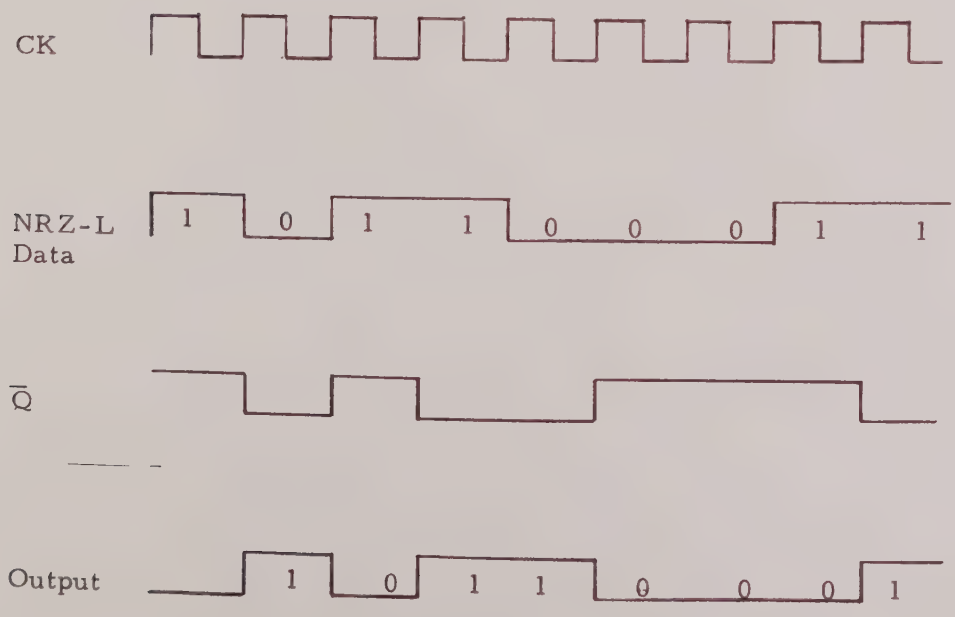
Figure 4-11. Equivalent Circuit, Code Conversion; Bi-Phase to NRZ-L

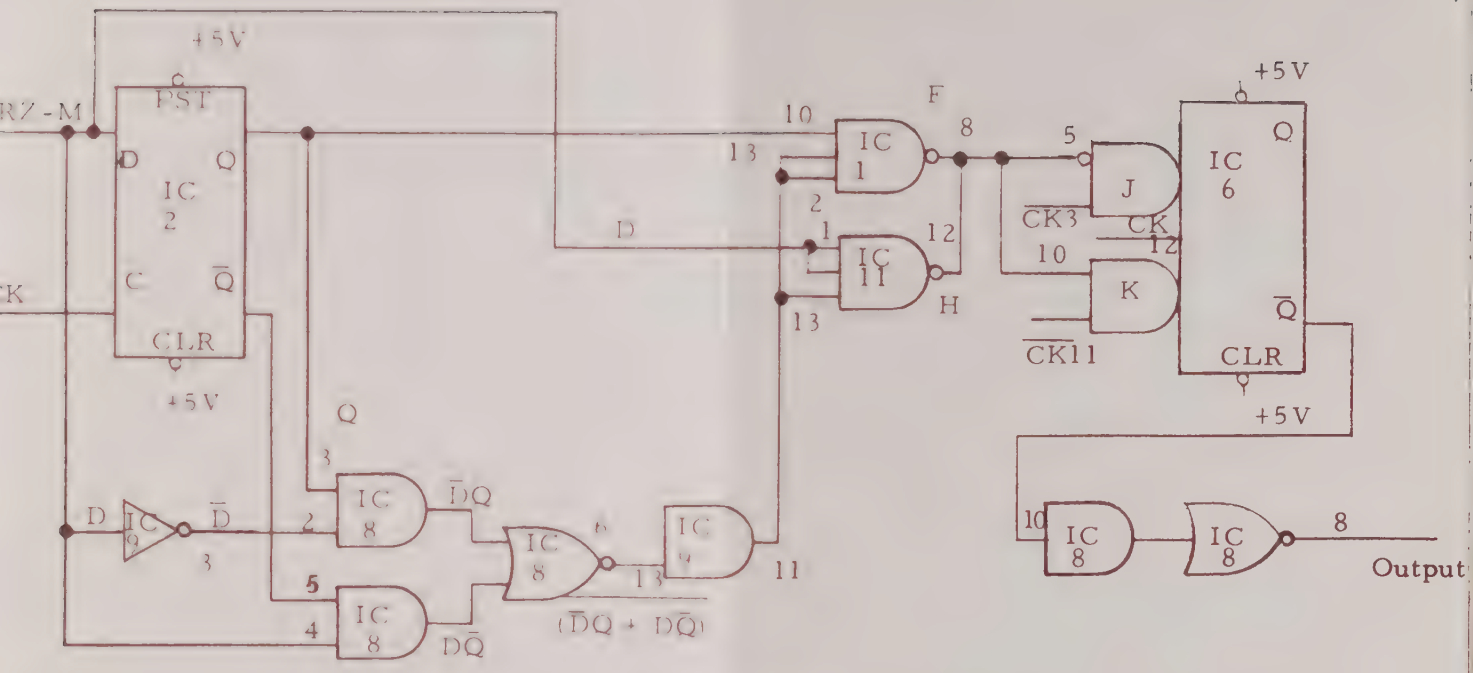
A

NRZ-L to NRZ-L



$\overline{NRZ-L}$ - Q output of IC-6 is used.





NRZ-S - employs the same equivalent circuit except the Q output of IC6 is used.

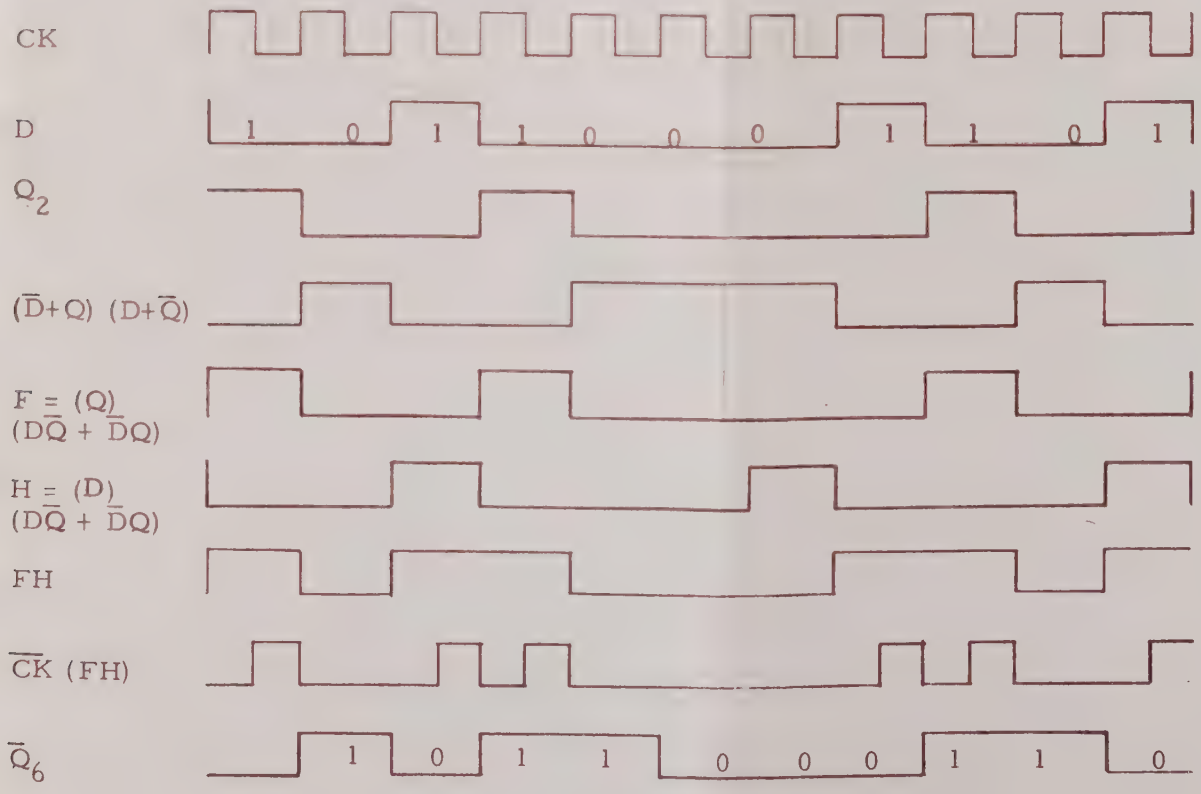


Figure 4-12.
Equivalent Circuits, Code Conversion, NRZ-M to NRZ-I

the $\overline{Q}$ level). The application of inverted data ($\overline{\text{NRZ-L}}$), therefore, requires in all cases a similar program except that the Q side of flip-flop 6 is selected.

b. NRZ-M - In order to convert NRZ-M to NRZ-L, it is necessary to sense transitions in the data, convert these to a high level and to convert all non-transitions to a low level. The equivalent circuit and the program used to derive it are given in Figure 4-12B. Transitions are sensed by IC-8 and IC-9 configured as an exclusive OR circuit. The output expression for the circuit is $\overline{D}Q + D\overline{Q}$ and since the Q output is data buffered by one clock cycle, an output is obtained on every transition. Compare the timing diagrams for D and ($\overline{D}Q + D\overline{Q}$). As with NRZ-L conversion the D and $\overline{D}$ program lines are used to select the Q or $\overline{Q}$ output from flip-flop 8, in this case the $\overline{Q}$ output. Not shown in Figure 4-12B is the generation of the system clock since the method is identical to that shown previously.

c. NRZ-S - The NRZ-S data is complemented NRZ-M. The conversion of NRZ-S, therefore, is identical to the conversion of the NRZ-M except that the Q output of flip-flop IC-6 is used.

d. RZ - To convert RZ data to NRZ-L it is necessary to expand all high levels by a half clock cycle without changing the low level data. Consider also that the bit synchronizer SBS-2 generates a VCO signal which is twice the frequency of the system clock. The data is ORed with buffered data (Q_2) and applied to flip-flop IC 6 where the $\overline{Q}$ output is used as the converter output. When serial RZ data is first applied to the converter, the initial state

of flip IC2B is indeterminate. If Q is initially high, the output is out-of-phase with the 2 clock input. The timing diagram given in Figure 4-11B illustrates that the Q output of flip-flop IC-6 is NRZ-L regardless of the clock phase. Therefore, the outputs of the code converter are CLOCK and $\overline{\text{CLOCK}}$ by definition and since all timing and triggering in the 4001 PCM System are relative to these signals, no ambiguities can occur.

As in the previous codes $\overline{\text{RZ}}$ is converted in the same manner as RZ except that the Q side of flip-flop IC-6 is applied to the output.

e. Bi-Phase-L - The conversion of Bi-Phase-L data to NRZ-L necessitates sensing the phase of high level signals with respect to clock. If a high level occurs during the first half of the clock cycle, a high level must be applied at the output. If the high level occurs during the second half of the clock cycle, a low level must be applied to the converter output. The equivalent circuit and the program used to convert Bi-Phase-L to NRZ-L is shown in Figure 4-11A. The first set of timing diagrams illustrates the operation when input data and VCO (2CK) are in proper phase. Signal $\overline{\text{CK}}$ is applied to both the J and K inputs of flip-flop IC-6. Since $\overline{\text{CK}}$ can only be high for one half of a cycle, it limits the setting and resetting conditions to a half cycle. If during this period, the data is high, the conditions for resetting exist. If on the other hand the data is low, the setting conditions exist and; on the next positive going trigger, the Q output goes high or low (or stay high or low) depending on which condition is satisfied.

In addition to code conversion, this circuit card contains the bit counter circuitry. The bit counter is a standard 4 stage parallel binary counter composed of JK flip-flops which counts to a value of 15. (Refer to drawing 075003). Resetting of the bit counter occurs by programming the desired last count (basic syllable length) on the program cards, or when the correlator causes NAND gate 14 IC-8 output to go low. In the former case, the counter is reset to 0000 (1st count) while a correlator reset sets the counter to 0010. When the programmed last count is achieved in the bit counter, the output of NOR gate 16 IC-8 is driven low causing the counter to reset and simultaneously causing the $\overline{Q}$ output of the D type flip-flop to generate an advance pulse to the Word counter.

The correlator applies two gates to the bit counter clear circuits (NAND IC-14) both of which must be high before resetting will occur. SD (Sync Detected) will go high whenever a synchronization pattern is detected, the other (Aperture or SEARCH) will go high whenever the system is in the SEARCH mode thereby resetting the bit counter on the next SD pulse. When the system is in a $\overline{\text{SEARCH}}$ mode; that is VERIFY, CHECK or LOCK, the line will go high only during those times at which the synchronization pattern is expected, and upon coincidence of the Aperture and SD pulse the bit counter is reset. In order to prevent false count during the clearing process, the Aperture or SEARCH line going high inhibits the clock thru NOR gate IC-16.

When a PCM format is being used which employs a periodic variable word length or to adapt the system to a greater than 16 bit word length format, the alternate syllable resetting circuits have been added. The alternate syllable length is programmed in a

similar fashion as the basic syllable length program lines, but the alternate syllable location is also programmed for the specific word in the word counter after which the word length is varied. When this count comes up NAND gate IC-18B will be driven to a low level inhibiting the resetting signal from NAND IC-21 while simultaneously enabling the resetting signal from NAND IC-20.

As an example, consider a format which contains periodic word lengths of 8 bits, 8 bits, 8 bits and 3 bits, throughout the frame. A BASIC SYLLABLE LENGTH of eight is programmed, an ALTernate SYLLable Length of 3, and ALTernate SYLLable LOCATION of 3 (the fourth count) on the program card. As the first word is shifted into the shift register the reset signal from the basic syllable length gates (IC-21) are enabled and reset the counter at the count of seven, an advance pulse is applied to the word counter and the second and third words are counted. Upon receipt of the third advance pulse, the word counter through NAND IC-18 will disable the basic syllable length resetting circuits; and enable the alternate syllable resetting circuitry which will reset the bit counter on the count of 2 (the third count).

The generation of the WINDOW pulses is accomplished by NAND gates IC-18A, 19A and 19B. The duration of the window is selected by the program card (window). The inhibition of NAND 19 and NAND 15 by the program will allow IC-19 to generate a window with a one bit duration. Programming A positive will enable NAND 19 and increase the window duration to 3 clock cycles. Similarly programming A & B to a high level will increase the WINDOW duration to 5 clock cycles. Observe that the WINDOW is generated for every word. The transformation of the WINDOW to the APERTURE which occurs only

at one specified time is, of course, that time at which a SYNChronization DETection is expected.

4.5.3 Data Storage and Control Assembly 070057

The NRZ-L serial data and clock output of the code converter is applied to the data storage and control assembly 070057. This assembly contains the first stage of the 33 stage shift register figure 4-13, and pattern recognizer, a 12 stage parallel storage register, a strobe generator and the logic to generate miscellaneous timing and control signal gates used throughout the balance of the system.

All stages of the shift register and pattern recognizer are identical and are described in paragraph 4.5.4.

The control circuitry contained on this assembly generates seven gating signals; three of which are used to gate the desired pattern recognizer, and four gates which are used to activate the appropriate error tolerance control logic contained on the Error Detector board (refer to logic drawing 075057). When the system is operating with any format code other than URC, flip-flop (IC-3) is held in the "Q" state with the grounded URC program line. The Q output of this flip-flop enables the gates associated with the Frame and $\overline{\text{Frame}}$ pattern recognizers, and the $\overline{Q}$ output disables the gate associated with the subframe pattern recognizer. When the format contains a unique recycling code (subframe sync), the URC program line is high and the state of flip-flop, IC-3, is controlled by the Search signal from correlator #1 and the last count of each frame. When the format contains a unique recycling code, the frame sync pattern is always located at the start of the frame whereas the subframe sync pattern can be in any other word location of the frame. Consequently, it is

only necessary to activate the frame pattern recognizer for the first word of each frame while the subframe pattern recognizer must be available for all remaining words of each frame. This is accomplished with flip-flop (IC-3) in conjunction with the SEARCH signal from correlator #1, and the LAST count FRAME signal from the word counter. When correlator #1 is in the SEARCH mode the SEARCH signal is high, and it holds flip-flop (IC-3) in the "Q" state to activate the frame pattern recognizers. Upon detection of the first frame sync pattern, correlator #1 is placed in the VERIFY mode; and the SEARCH signal goes low to allow flip-flop (IC-3) to be placed in the $\overline{Q}$ state to activate the subframe pattern recognizer. The flip-flop remains in this state until the last count frame signal, corresponding to the last word of each frame, goes high. At this time, the flip-flop is placed in the "Q" state for one word at a time. This sequence is repeated for each frame.

In addition to controlling the gating of the pattern recognizers, flip-flop (IC-3) is also used with the SEARCH signals from both correlators to control the four error detector gate signals (EDGTA, EDGTB, EDGTC and EDGTD). These four gates are used to select the appropriate error tolerance control logic contained on the Error Detector Board. Gates A and B are associated with the error tolerance allowed in the frame sync pattern in the SEARCH and $\overline{\text{SEARCH}}$ modes, respectively. The actual selection of allowable errors is determined by the setting of the MAIN FRAME SYNC STRATEGY Es and $E\overline{s}$ thumbwheel switches on the front panel. Gates C and D are associated with the error tolerance allowed in the subframe sync pattern in the SEARCH and $\overline{\text{SEARCH}}$ modes respectively. The number of allowable errors is selected by the program card. Referring to the logic drawing 075057, gate A or B is activated simultaneously

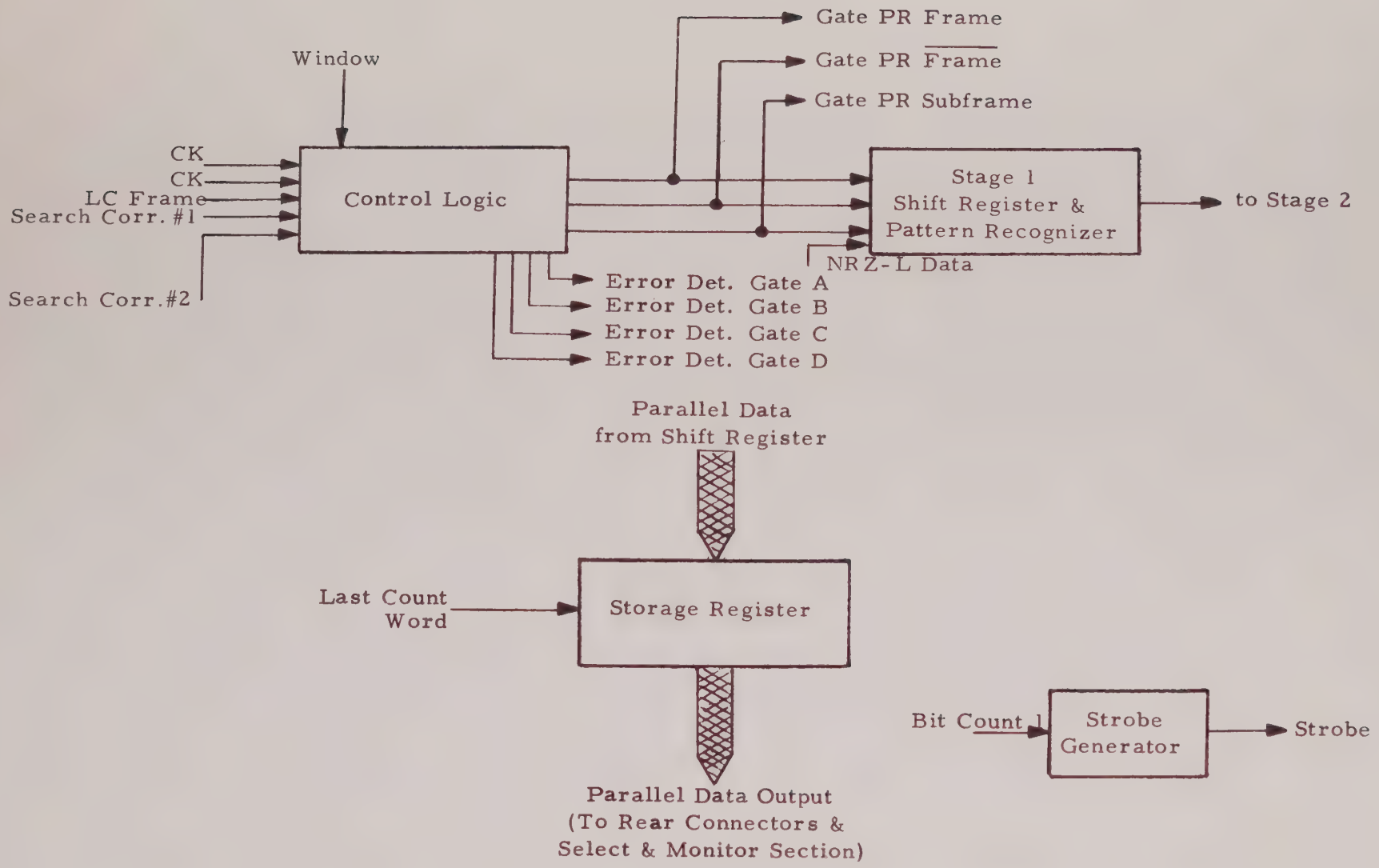


Figure 4-13. Block Diagram, Data Storage & Control Ass'y. 070057

with the frame pattern recognizer; while gate C or D is activated with the subframe pattern recognizer.

Also included on this circuit board is the 12 stage parallel storage register which accepts the shift register output and stores each word for one word length. The load pulse is derived from the bit counter (LAST COUNT BUFF). The clear input of each flip-flop is programmable to allow the number of stored bits to vary from 0 to 12 and forces all unused stages to the $\overline{Q}$ state; thereby, providing logical zeros for all unused bits of the parallel data.

A D type flip-flop (IC-25) and a NAND gate (IC-22), also located on this board, are used to generate a strobing pulse (CT1 BUFF) for the D/A conversion and external timing. Since the data contained in the parallel register is stored for one word length, the first count from the bit counter for the succeeding word is used to guarantee the generation of the strobe after all data has had sufficient time to settle.

4.5.4 8 Bit Shift Register and Pattern Recognizer Assembly 070053

There are four 070053 circuit boards contained in the 4001 PCM System and they are located in positions 11, 12, 13 and 14 of the card file. Each of these boards is interconnected to form one 33 bit shift register and pattern recognizer (the first stage and least significant bit of the register is located on the DATA STORAGE and CONTROL ASSEMBLY 070057). The logic diagram for one stage of the shift register and pattern recognizer is shown in figure 4-14. The flip-flop shown contains one bit of data at any specific time which is derived from the Q output of the preceding stage. Other external applied signals are four programmable lines, clock, and

three pattern recognizer gating signals (PR FRAME, PR $\overline{\text{FRAME}}$, and PR SUBFRAME).

The purpose of the pattern recognizer is to recognize synchronization codes (frame or subframe) when they appear in the serial data train. This is accomplished by sensing the output of each flip-flop and if the output agrees with the pre-programmed pattern to indicate this agreement by driving each output line low. Three pattern recognizers are used and each is gated at the appropriate times to recognize the programmed frame sync pattern, the compliment of the programmed frame sync pattern, or the programmed subframe sync pattern. In each bit recognizer the external gates and programs perform the following functions to accomplish this.

a. Program lines IC4A and IC4B - These program lines are used to select the desired frame sync pattern, and its compliment. A ground (punch) on the IC4A program line selects a "1" for this particular stage, and a ground on the IC4B program line selects a "0". Note that these two program lines are also connected to the opposite gates of the pattern recognizer associated with the $\overline{\text{FRAME}}$ pattern recognizer, therefore, this pattern recognizer is simultaneously programmed to detect the complimentary sync pattern. When the programmed bit is present in the corresponding stage of the shift register, the output of pattern recognizer gates go low. A low level on each of the pattern recognizer output lines is an indication to the Error Detector that the programmed sync pattern is present in the proper location of the shift register. If all 33 storages of the shift register are not required to program a sync pattern, the unused stages must be programmed for a "don't care" condition. This is accomplished

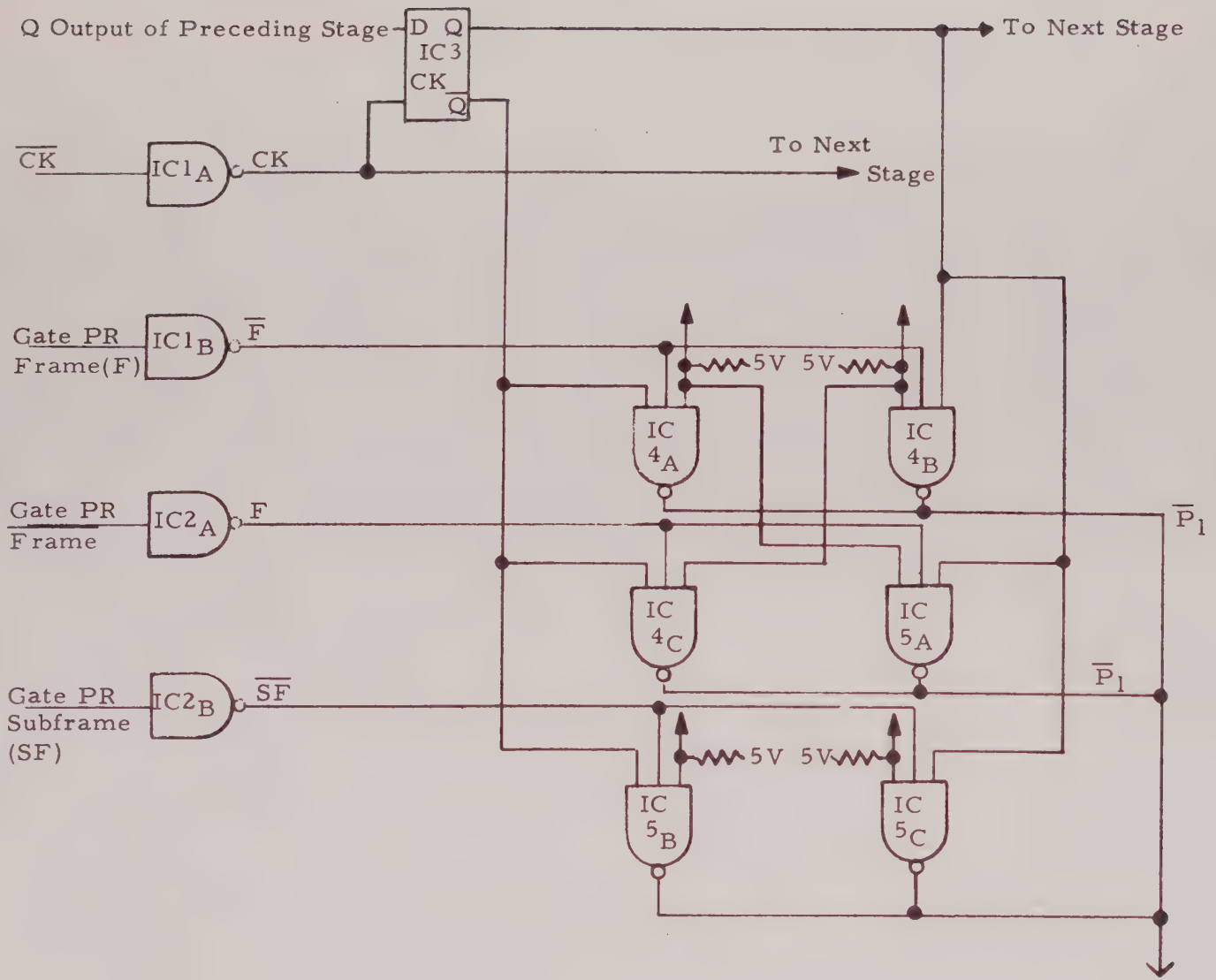


Figure 4-14. Typical Stage of Shift Register and Pattern Recognizer Ass'y.

by leaving both program lines high (no punch). Since the two gates of each pattern recognizer stage function as an "OR" gate, the output is low for both states of the shift register.

b. Program Lines IC5B and IC5C. These program lines are used to select the desired subframe sync pattern. The logic function is identical to that of the frame sync pattern recognizer.

c. GATE PR FRAME and GATE PR $\overline{\text{FRAME}}$. Those signals are enabling gates which allow the pattern recognizer to sample the output of the flip-flop for the frame sync pattern. The GATE PR FRAME, and GATE PR $\overline{\text{FRAME}}$ gate their respective pattern recognizers at clock and $\overline{\text{clock}}$ times respectively when the system is programmed for Frame Synchronization, Frame Alternating Complement, or Frame Code Complement. When the system is programmed for unique recycling code, these signals are only activated in the frame SEARCH mode; or during the first word of each frame (the expected time for the frame sync pattern). At all other times, the frame and $\overline{\text{frame}}$ pattern recognizers are inhibited.

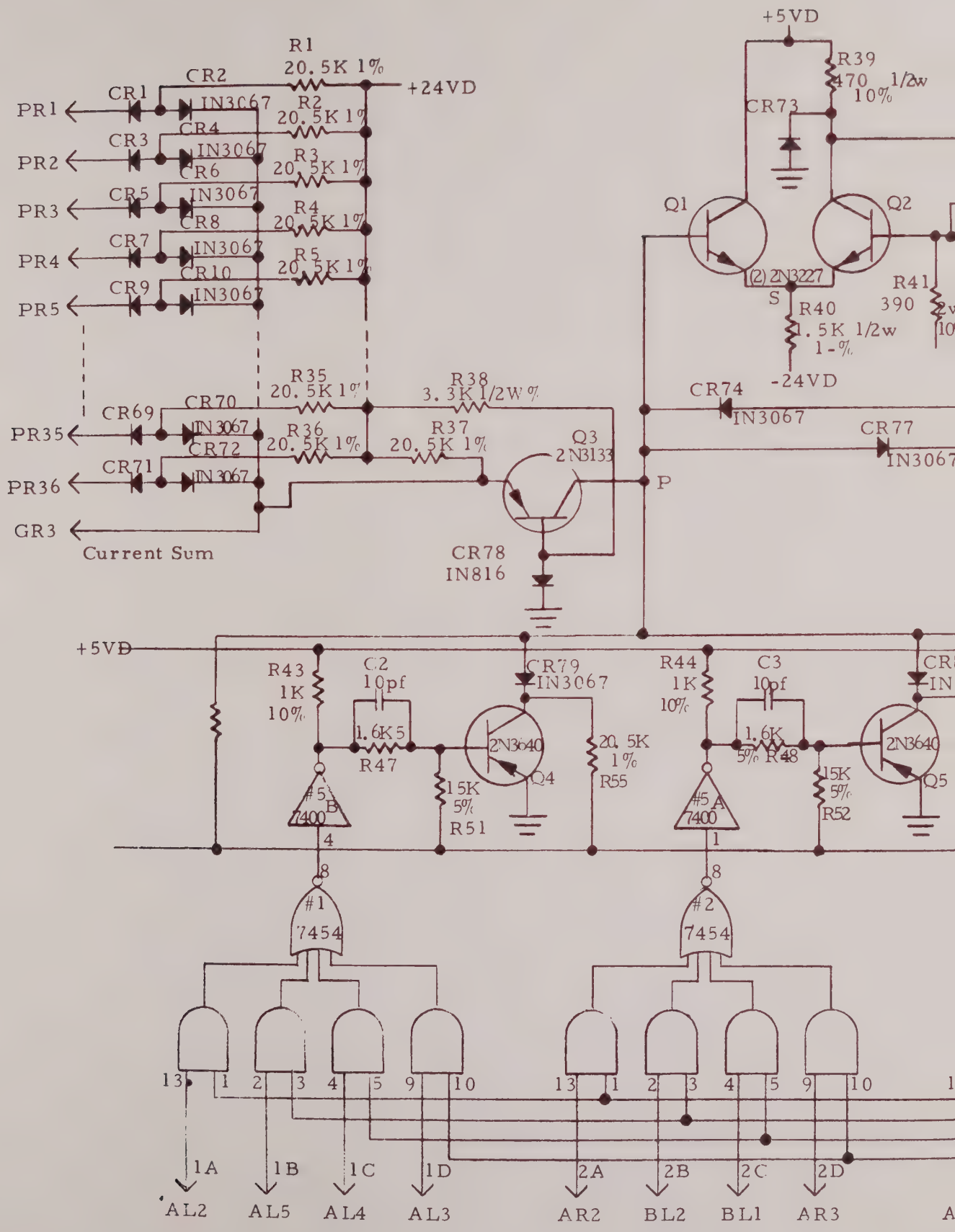
d. Pattern Recognition Gate (Subframe) - This is an enabling gate to the subframe pattern recognizer NAND gates (IC5B and IC5C). The gate cycles every clock period except during the frame SEARCH mode, and the first word of each frame. At these times, the input goes to a high level to disable the subframe pattern recognition NAND gates.

4.5.5 Error Detector Assembly 071022

The output of each bit recognizer contained on the Shift Register and Pattern Recognizer Assembly is applied to the error detector assembly 071022. The error detector, functionally a part of the pattern recognizer, evaluates the overall pattern formed by each bit recognizer and if found to be a synchronization pattern, generates a pulse which is applied to the correlator.

The overall schematic for the Error Detector may be found on drawing 071022, while a simplified version is given in Figure 4-15. The bit recognizer outputs are applied to the error detector inputs PR1 through PR33 (inputs 34, 35, and 36 are not used in the 4001 PCM System and are grounded). Consider a time in which each stage of the shift register is in the incorrect state, that is, no stage of the shift register contains a sync pattern bit. At this time, the output of each bit recognizer will be a high level. Transistor Q3 will be conducting heavily at approximately 33 ma. Approximately 1.7 ma of this current will flow through R42 with the balance flowing through CR77 and R41. Diode CR75 and CR76 are used to set a reference level of -1.4 volts at the base of Q2. The voltage across CR77 increases until a forward bias is obtained, and since the cathode of CR77 is fixed (at -1.4 V DC) -0.7 V DC is developed at the anode to be transferred through emitter follower Q1. Transistor Q2 is cutoff, and hence the Q outputs of flip-flops 6A and 6B are low levels which are used as indications that the synchronization pattern is not present in the shift register.

As data is shifted into the shift register, the bit recognizers start to sense correct (sync pattern) bits, and the current output of Q3 will increase and decrease depending on the number of


+5VD
R1
20.5K 1%
CR2
CR1
IN3067
+24VD
PR1
R2
20.5K 1%
CR4
CR3
IN3067
PR2
R3
20.5K 1%
CR6
CR5
IN3067
PR3
R4
20.5K 1%
CR8
CR7
IN3067
PR4
R5
20.5K 1%
CR10
CR9
IN3067
PR5
R39
470 1/2w
10%
CR73
Q1
Q2
(2) 2N3227
S
R40
1.5K 1/2w
1-%
-24VD
R41
390
R35
20.5K 1%
R38
3.3K 1/2W %
CR74
IN3067
CR77
IN3067
CR69
CR70
IN3067
PR35
R36
20.5K 1%
CR72
R37
20.5K 1%
Q3
2N3133
P
CR71
IN3067
PR36
GR3
Current Sum
CR78
IN816
+5VD
R43
1K
10%
C2
10pf
CR79
IN3067
R44
1K
10%
C3
10pf
1.6K 5%
R47
2N3640
Q4
20.5K
1%
R55
#5B
7400
4
15K
5%
R51
#5A
7400
1
15K
5%
R52
Q5
1.6K
5% R48
8
#1
7454
#2
7454
13
1
2
3
4
5
9
10
1A
1B
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AR2
BL2
BL1
AR3

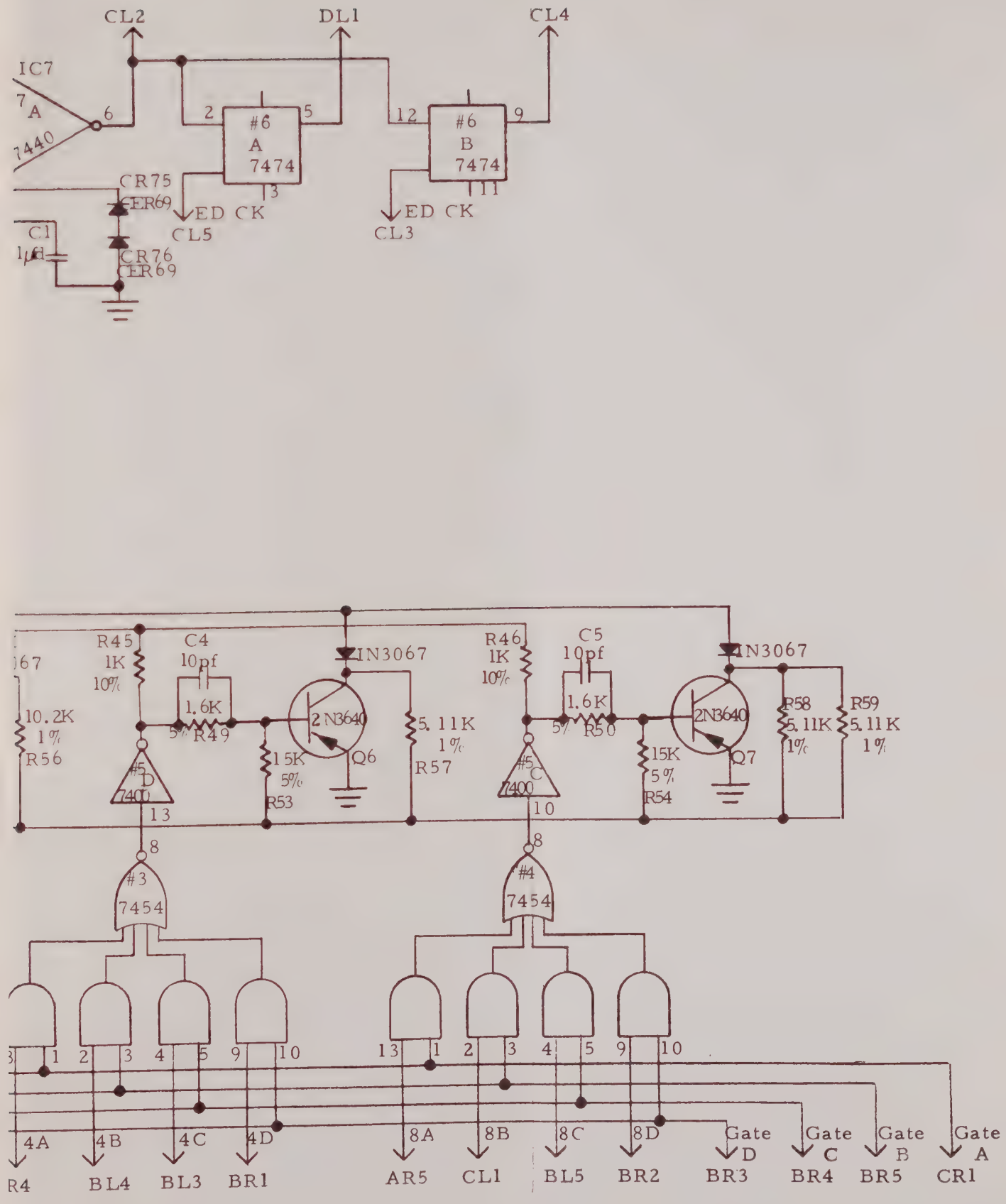


Figure 4-15. Error Detector, Simplified Schematic

correct bits sensed by the bit recognizers. As long as the Q3 output current exceeds 1.7 ma, however, no change will occur in the state of Q2. When the correct synchronization pattern appears in the shift register, all bit recognizer outputs will go low simultaneously; causing all current to be shunted from the emitter of Q3 (except approximately 1.2ma). When the current value drops below 1.7ma, the difference is drawn thru CR75 and CR76. In the process, a forward biasing voltage is developed across CR74 of approximately -2.1 V DC which, when transferred to node S forward biases Q2, turning it on and causing the outputs of flip-flops 6A and 6B to go high indicating a synchronization pattern has been detected.

The circuitry associated with Q4 through Q7 has been provided in order to allow a given number of errors in the sync pattern yet still be recognized as a valid pattern. When the output of inverter 5B is low as will be the case when the AND gates are not satisfied, Q4 is biased on to reverse bias CR79. Satisfaction of the input conditions of at least one of the AND gates causes inverter B5 to go to a high level which cuts off Q4, forward biasing CR79; and drawing an additional 1.1 ma from node P. Since the amount of additional current drawn from P is dependent on R55, R56, R57, R58 and R59, the turning off of transistors Q4 thru Q7 increases the current drain demand of the R42 network. The overall effect is that fewer bit recognizers need to go to a low level before Q2 is turned on. An error tolerance has then been added to the system.

The satisfaction of the input conditions to the AND gates is obtained through the thumbwheel switches on the front panel (e_s and $e_{\bar{s}}$) for frame error tolerances and the FORMAT STORAGE CARD for subframe error tolerances. Since the Error Detection is used for both frame and subframe sync indications, the error tolerance circuitry must be time shared if frame and subframe strategies are to be independent. For this reason, gates ABC and D have been added. These gates generated in the Data Storage and Control Logic Assembly 070057, are used as timing signals which goes to high levels at the indicated times resulting in different error tolerances being incorporated according to the operating mode and sync pattern being detected.

4.5.6 Format Counter Assembly 070047

This assembly is used both as a word counter and frame counter (when installed) in the 4001 PCM System. The word counter assembly is located in card file slot 18 and the assembly used as a frame counter is located in card file slot 19. The format counter assembly or word counter upon receipt of an ADVance pulse from the bit counter, counts each word of a frame; and supplies word identification information (figure 4-16) to the select and monitor section of the 4001 PCM System, to external word selectors, and peripheral equipment.

The format counter circuits consist of 3 independent four stage parallel counters (Section I, II and III) which thru appropriate programming may be interconnected to form a binary coded variable radix counter. The most commonly encountered configurations are as a binary or binary coded decimal counter (Refer to Drawing 075047). The advance pulse from the bit counter is applied to

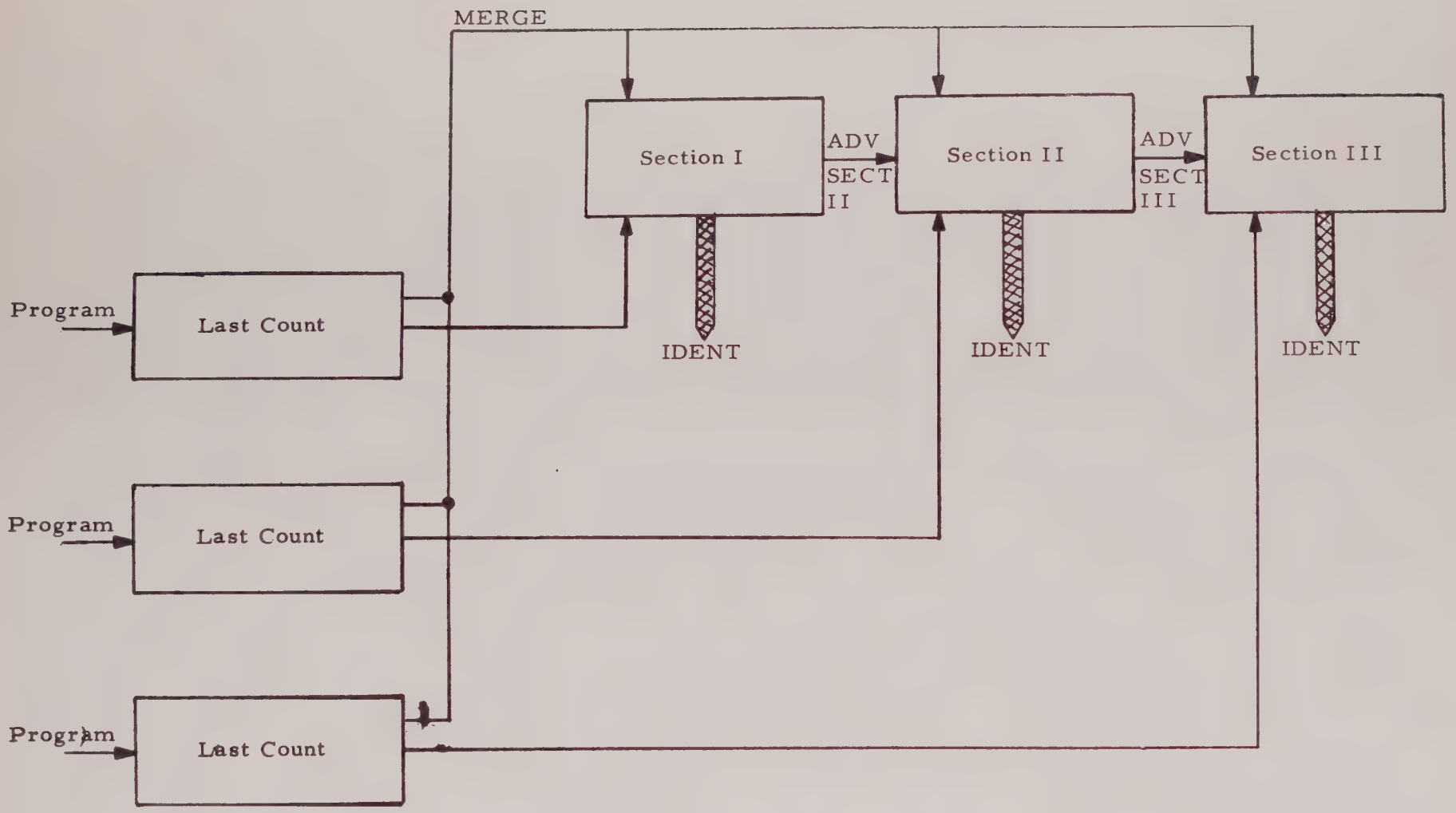


Figure 4-16. Block Diagram, Format Counter Ass'y. 070047

all trigger inputs of the JK flip-flops. Programming the last count of any derived counter is accomplished in an identical fashion as in the Bit Counter (through NOR gates 11, 12, and 14). Two additional program lines are added to configure stages as desired. Programming high levels on ADVance SECTion 2, and ADVance SECTion 3 on the FORMAT STORAGE CARD allow the last count of stage 1 to be applied to the J and K gates of Section II; and similarly with section III resulting in three series 4 stage counters.

The three independent stages can be configured as binary or BCD counters with the BCD program lines associated with each section. The independent sections function as BCD counters if the BCD program line is programmed high (no punch), and as a binary counter if the BCD program line is programmed low (punch).

The merge 1 and 2, and merge 2 and 3 program lines are used to combine the last counts of the independent sections of the format counter. Thus, an eight or twelve-stage register is formed. When the merge lines are programmed high (no punch); the independent sections of the format counter functions as straight binary or BCD counters as determined by the programming of the BCD program lines, and the cycle rate (last count) corresponds to the combined last counts of the independent sections.

4.5.7 Correlation Assembly 070058

The error detection generates a sync detected signal each time the programmed sync pattern is detected. The first detected pattern is used to reset the bit and format counters to a specific count. If

the dectected pattern is the true sync pattern, it is detected again in the following frame at a pre-determined bit time. The expected bit and word are determined by a window signal generated at the word rate by the bit counter, and the first word of the frame. The first word of the frame is derived from the LAST COUNT FRAME signal from the word counter.

If these three pulses are generated simultaneously, proper format synchronization is obtained (or maintained). If not, then proper format synchronization is not obtained (or being maintained) and appropriate steps must be taken to CHECK, VERIFY, or SEARCH for proper sync. These steps are performed by the Correlator Assembly 070058. A block diagram of the Correlator Assembly is shown in Figure 4-18. The Error Detector, upon receipt of the proper signals from the Pattern Recognizers, will generate Sync Detected pulses (SD BUFF and $\overline{\text{SD}}$ BUFF); and apply them to the sync detected pulse normalizer circuits of the correlator. Sync detected signals will appear depending on the synchronization code (frame synchronization, frame alternating complement synchronization, or frame code complement synchronization) delayed by 1 or 1-1/2 clock periods. It is the function of this synchronization detector generator to normalize these delays to 1-1/2 clock cycles so that proper correlation may be obtained.

The WINDOW generated in the Bit Counter and Code Converter Assembly is applied to the aperture generator. The window which is 1, 3, or 5 bits long (programmed) comes up at the word rate. The aperture generator using the WINDOW, word and frame information; generates a pulse at the expected time of the sync pattern. One exception to this is when the system is operating in the SEARCH

mode, in which case the aperture generator will be continuously enabled to allow the first detected sync pattern to transfer the system to VERIFY.

The correlator accepts the sync detected pulse output (normalized) which indicates that a synchronization pattern is detected; and accepts the aperture (from the aperture generator) which indicates the time synchronization pattern is expected. Signals indicating detection of a sync pattern, or the absence of a detected sync pattern at the expected time is applied to the mode control logic; where it is used to maintain or change the operating mode of the system.

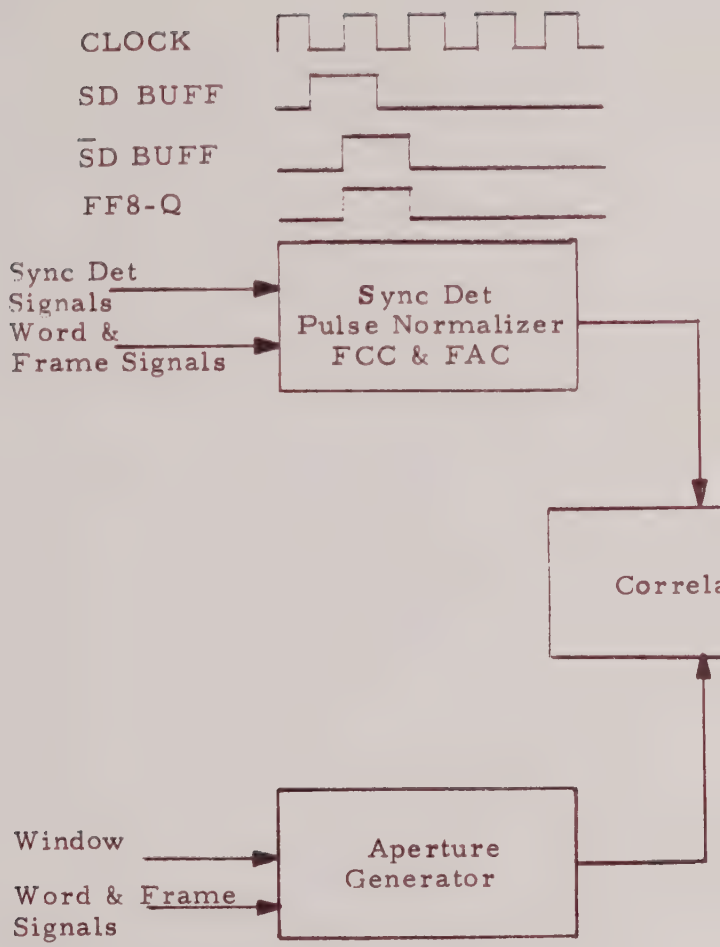
The VERIFY accumulator may be set to any desired number of successive correct sync patterns from 0 to 15 by the front panel mounted switch. Upon accumulation of the set number of successive correct sync patterns (only 1 incorrect pattern returns the system to SEARCH). The system is transferred to the LOCK mode where it will remain until an incorrect sync pattern is received from the correlator. The mode control logic then transfers the system to CHECK where any correct pattern returns the system to LOCK and the accumulation of up to 15 incorrect patterns (front panel mounted thumbwheel E_c) will transfer the system to SEARCH. The logic diagram for the correlator assembly may be found on drawing 075058.

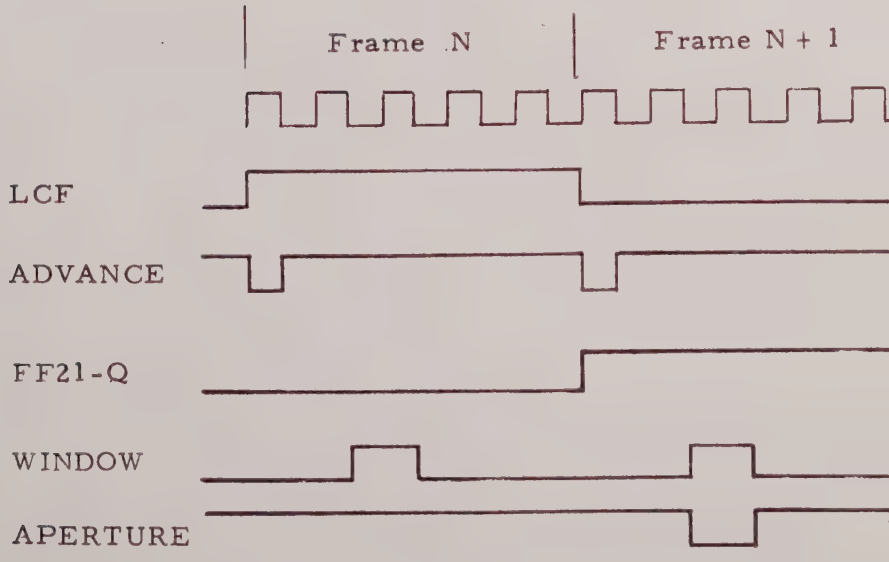
The sync detected pulse normalizer is comprised of IC1 thru IC6 and IC8. (Field of drawing C4). If the system is in the SEARCH mode, the first sync detected pulse (SD BUFF) from the Error Detector presets flip-flop IC5 and generate an SD signal at the output of flip-flop IC8 which causes the system to go to VERIFY.

If FAC synchronization is being used, the arrival of sync detected pulses will alternate between the SD BUFF and $\overline{SD}$ BUFF signals. This relationship is shown in the timing chart on Figure 4-17. Note that only one of these pulses is present in a given frame, (i.e. if SD BUFF occurs in frame N, $\overline{SD}$ BUFF will occur in Frame N + 1).

With FAC synchronization employed NAND gate IC-2 will be programmed high allowing the D input to flip-flop IC5 to go high or low as dictated by LAST COUNT FRAME (LCF) and its Q output. Consequently, the 8 input to flip-flop IC8 alternates between the SD BUFF; and the $\overline{SD}$ BUFF signals at the frame rate. The overall result can be seen in the timing charts of Figure 4-17, which illustrates that regardless of the timing of the sync detected pulse, the flip-flop IC8 Q output always occurs on the same relative clock cycle every frame. A similar reaction occurs with a frame code complement synchronization pattern.

The aperture generator of figure 4-17 consists of IC4, IC21 and IC17 (field of drawing D-4, 3). The last count frame signal (LCRR) is derived from the word counter, and is a positive pulse one word wide that is time-coincident with the last word of each frame. This signal is buffered by one word with the advance (ADV) signal through flip-flop IC21 to provide a positive pulse one word wide that corresponds to the first word of every frame. The Q output of this flip-flop is used with the WINDOW signal to generate the APERTURE which is the expected bit time of the sync pattern.


CLOCK
SD BUFF
$\overline{\text{SD BUFF}}$
FF8-Q
Sync Det Signals Word & Frame Signals
Sync Det Pulse Normalizer FCC & FAC
Correla
Window
Word & Frame Signals
Aperture Generator


Frame N
Frame N + 1
LCF
ADVANCE
FF21-Q
WINDOW
APERTURE

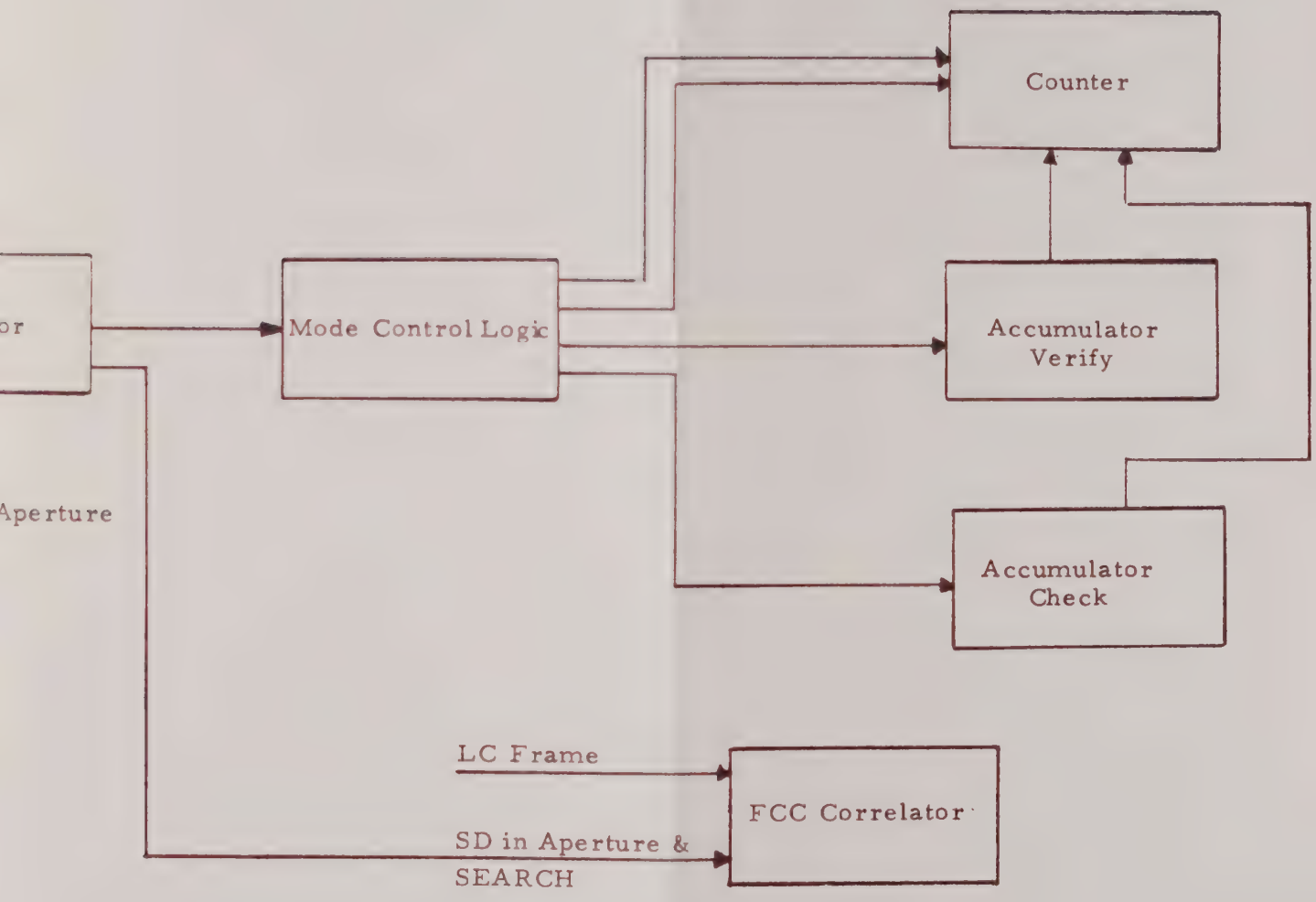


Figure 4-17. Block Diagram, Correlator I

The correlator of Figure 4-17 consists of JK flip-flop IC18. Since the K input to this flip-flop is the LC BUFF signaled and it is triggered with the $\overline{CK}$ signal, it is normally in the $\overline{Q}$ state. When the system is in the SEARCH mode, this flip-flop is set to the Q state upon receipt of the first SD signal. When the system is in any mode except SEARCH, this flip-flop sets to the Q state only when the SD signal occurs at the expected time (APERTURE). Upon receipt of the first SD signal, the $\overline{Q}$ output of flip-flop IC18 presets flip-flop IC21, which (part of the mode control logic) places the system in the VERIFY mode. Simultaneously, the SD and Aperture signals are used to reset both the bit counter and the word counter. After being reset, the counters free run at the bit rate of incoming data. If the first sync pattern detected is the sync pattern, it occurs in the following frame time coincident with the aperture signal. If the first sync pattern detected was not the true sync pattern, flip-flop IC21 is reset to the $\overline{Q}$ state and the system returns to the SEARCH mode.

The mode control logic of Figure 4-18 is located in the field of drawing B2 of 075058. The Master Reset Switch, when actuated, clears flip-flop IC21 and IC22 to the $\overline{Q}$ state resulting in the system being automatically placed in SEARCH. Eventually a sync pattern is detected and flip-flop IC21 $\overline{Q}$ output goes low which forces IC21 to the Q state, places the system in the VERIFY mode, and allows the counters (IC23 and IC24) to count successive correct sync patterns at the expected time. If a sync pattern is not detected in the aperture while the system is in the VERIFY mode flip-flop IC21 resets to the $\overline{Q}$ state and the system returns to the SEARCH mode, the counters clear, and the process is reinitiated. After a

given number of true Sync Detected patterns (programmable from 0 to 15), the VERIFY accumulator supplies a high level to the J input of flip-flop IC22. This allows the "Q" output to go high on the next clock signal to illuminate the LOCK lamp, and place the system in LOCK.

The correlator continues looking for the sync pattern at the expected time while the system is in the LOCK mode, and the first incorrect or missing sync pattern at the expected time resets flip-flop IC22 to the $\overline{Q}$ state to place the system in the CHECK mode. If a given number of incorrect patterns are detected, the CHECK accumulator supplies a low level to the D input of flip-flop IC21 causing the system to revert to the SEARCH mode, and reinitiating the entire sequence. If during the accumulation of incorrect patterns in the CHECK mode; one correct (true) sync pattern is detected, flip-flop IC18 presets flip-flop IC22 and returns the system to the LOCK mode.

The VERIFY and CHECK accumulators consist of four flip-flops and programmable logic used to determine the last counts in the VERIFY and CHECK modes independent of each other. This circuit is similar to the bit counters discussed in paragraph 4.4.2.

The Frame Code Complement Correlator is located in the field of drawing D1. Upon the receipt of a SD in aperture and a $\overline{SD}$ buffered pulse (complementary Sync pattern) from the main frame correlator flip-flop IC10 presets to place the subframe sync status in LOCK.

4.5.8 Correlator II Assembly 070059 (Models -110, -111 only)

The Correlator II Assembly (figure 4-18) is used for the synchronization of sub-frame data when the synchronization method is either a Unique Recycling Code (URC) or a Subframe Identification Pattern (SFID). The assembly, therefore, will be found only on the 4002-110 and -111 models.

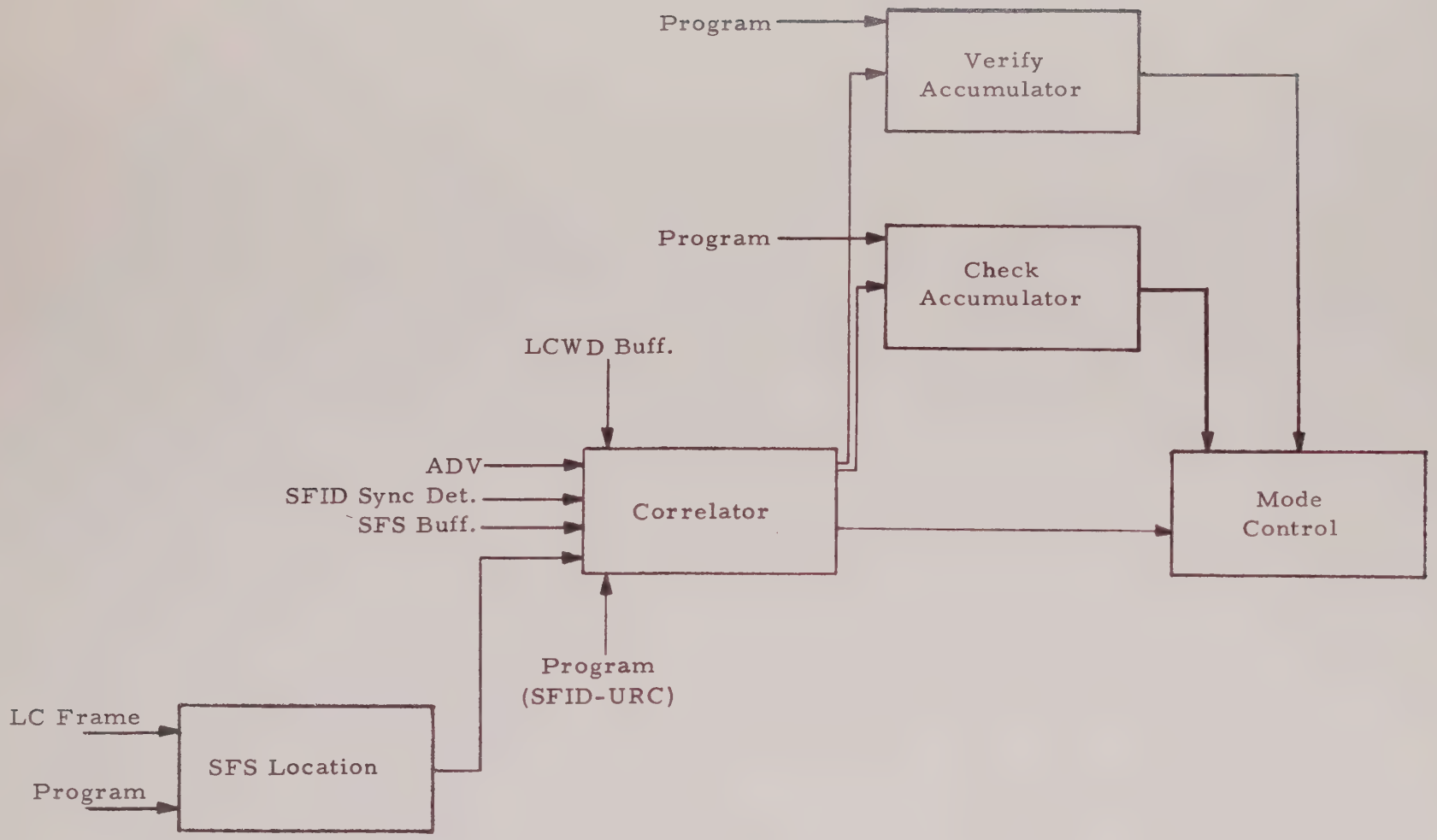


Figure 4-18. Block Diagram, Correlator II Assembly 070059

The operating modes of subframe synchronization are essentially the same as the Main Frame; that is, SEARCH, VERIFY, CHECK and LOCK. The only significant difference is that the main frame operating mode will maintain top priority over both operating modes. If the main frame operating mode transfers from CHECK to SEARCH, the subframe operating mode will automatically be placed in SEARCH.

The logic diagram of the Correlator II assembly is given on drawing 075059. Circuits IC23, 24, 25 and 26 comprise a programmable VERIFY and CHECK accumulator identical to the accumulator used on the Correlator I Assembly. Circuits IC2, 3, 4, 5, 6, 7 and 10 are used to program the word location of the subframe synchronization pattern. The program lines are used to identify the specific word of a frame in which the subframe sync pattern is located. When that word identification is contained in the word counter, NAND IC-5 goes low causing NAND IC-7 to go to a high level for one word which corresponds to the subframe sync location. Flip-flop IC10 is set to the Q state at the start of each frame and resets to the $\overline{Q}$ state at the end of the programmed subframe word location. This avoids the necessity of reading both the Q and $\overline{Q}$ outputs of the word counter to locate the subframe synchronization pattern. For example, if the subframe sync pattern is located in word 5 of every frame, the SFS location is programmed 0101 (decimal 5). The "0"s constitute a "don't care" function, and the output of NAND IC-5 goes to a low level; not only when the word counter reads 0101, but also on the count of 0111, 1101 and 1111 (ignoring the effects of stage II and stage III of the word counter) However, only the first count transfers the flip-flop, IC10, to $\overline{Q}$ where it remains until Last Count Frame toggles the flip-flop back to Q.

Considering the operation of the Correlator II Assembly when a Unique Recycling Code (URC) is being used as a subframe synchronization pattern, the sequence of operation is as follows.

The main frame operating mode is placed in SEARCH causing the subframe operating mode to be transferred automatically to SEARCH. This is accomplished through RESET -2 (field of drawing C2) which will go to a high level whenever the main frame operating mode is SEARCH. This action clears flip-flops IC20, IC16, which is the SEARCH mode for Correlator II. After the main frame correlator returns to a $\overline{\text{SEARCH}}$ operating mode, the subframe correlator (II) will remain in SEARCH until a sync detected signal (SD) appears on the input to NAND IC6-4 at the expected time (that is, when the subframe sync pattern is located in the shift register which is indicated by the output NAND IC7-10 going to a high level). When this occurs, the $\overline{Q}$ output of flip-flop IC9 goes to a low level causing the correlator to transfer to the VERIFY mode (by the presetting of the flip-flop IC16). The accumulator counters are now enabled allowing the accumulation of the programmed number of correct sync patterns prior to transferring to LOCK. As in the Correlator I Assembly, one incorrect pattern will revert the operating mode to SEARCH.

Upon the accumulation of the programmed number of correct patterns, NAND IC25 goes to a high level placing the subframe operating mode to LOCK where it remains until an incorrect subframe sync pattern allows flip-flop IC20 to transfer the operating mode to CHECK. (LC BUFF enables the K gate, and since the PST gate is at a high level; the flip-flop toggles). The accumulation of the programmed number of incorrect sync patterns drives the D input to flip-flop IC16 low to return the operating mode to SEARCH while one correct sync pattern causes the PST gate (to flip-flop IC20) to go to a low

level; thus returning the system to the LOCK mode.

If a subframe identification code is used, the SFID PROG line is programmed to a high level which disables flip-flops IC8 and IC9. The $\overline{\overline{SFS}}$ BUFF (not subframe sync) goes to a high level at the expected sync time, that is, when the SFID is in the proper location of the register. The PATT DET (pattern detected) signal is the SFID equivalent to the SD pulse, that is, the PATT DET line goes to a low level when the SFID pattern compares with the contents of the frame counter. Thereafter, the operation of the Correlator II Assembly is the same as for a URC sync pattern.

4.5.9 SFID Synchronizer Assembly 070052 (-111 Model only)

The Subframe Identification (SFID) method of subframe synchronization is generally adopted to place a unique count within the transmitted data for identification of subframe. This feature prevents waiting for specific patterns to appear at subframe rate to achieve subframe synchronization.

Figure 4-19 is a functional block diagram illustrating the operation of the SFID sysnchronizer. The specific word of the main frame in which the SFID pattern is located, is programmed on the FORMAT STORAGE CARD (SFS location). Since the SFID pattern may be somewhat shorter than the basic syllable length, the first and last bit location of the SFID is also programmed (BIT START - BIT STOP). In the SFID synchronizer this information is used to initiate a clock to the shift register at the precise time at which the SFID pattern is ready to be shifted into the SFID shift register. The clock is turned off at the precise moment that the entire SFID pattern is located in the register. A comparison is then made between the contents of the register and the contents of the frame counter which

should be in agreement. If the contents of the register agree, the comparator generates a signal, indicating that an SFID pattern is detected. If the contents disagree, the comparator generates a clock to the frame counter which advances the count until an agreement is reached.

The logic diagram for the SFID synchronizer assembly may be found in drawing 075052. Upon receipt of the SFS location signal and the bit start signal from word and bit counters, respectively, flip-flop IC21 is transferred to Q which allows $\overline{CK}$ to toggle the shift register (IC7 thru IC10) thru IC13.

NAND gates IC3 thru IC6 function as a comparator. When the shift register is shutdown through the bit stop circuitry, the contents are applied to one input of these NAND gates while the contents of the frame counter are applied to the other. Since the true side of the shift register is being compared to the complementary side of the frame counter stages and vice versa, disagreement on the input side of the NAND gates is obtained when the frame counter and shift register are in agreement (synchronization). Furthermore, both the Q and $\overline{Q}$ outputs of the register must be read if both "1"s and "0"s are to be compared.

When the SFID pattern is in the register; and compared to the contents of the frame counter, a low level from the comparator signifying no synchronization is applied to the input of NAND gate IC12 driving it high and allowing $\overline{CLOCK}$ to be applied to the frame counters through IC13 and IC26. The frame counters are updated at clock rate until the contents of the shift register agrees with the co... of the frame counter. When this occurs the next frame advances

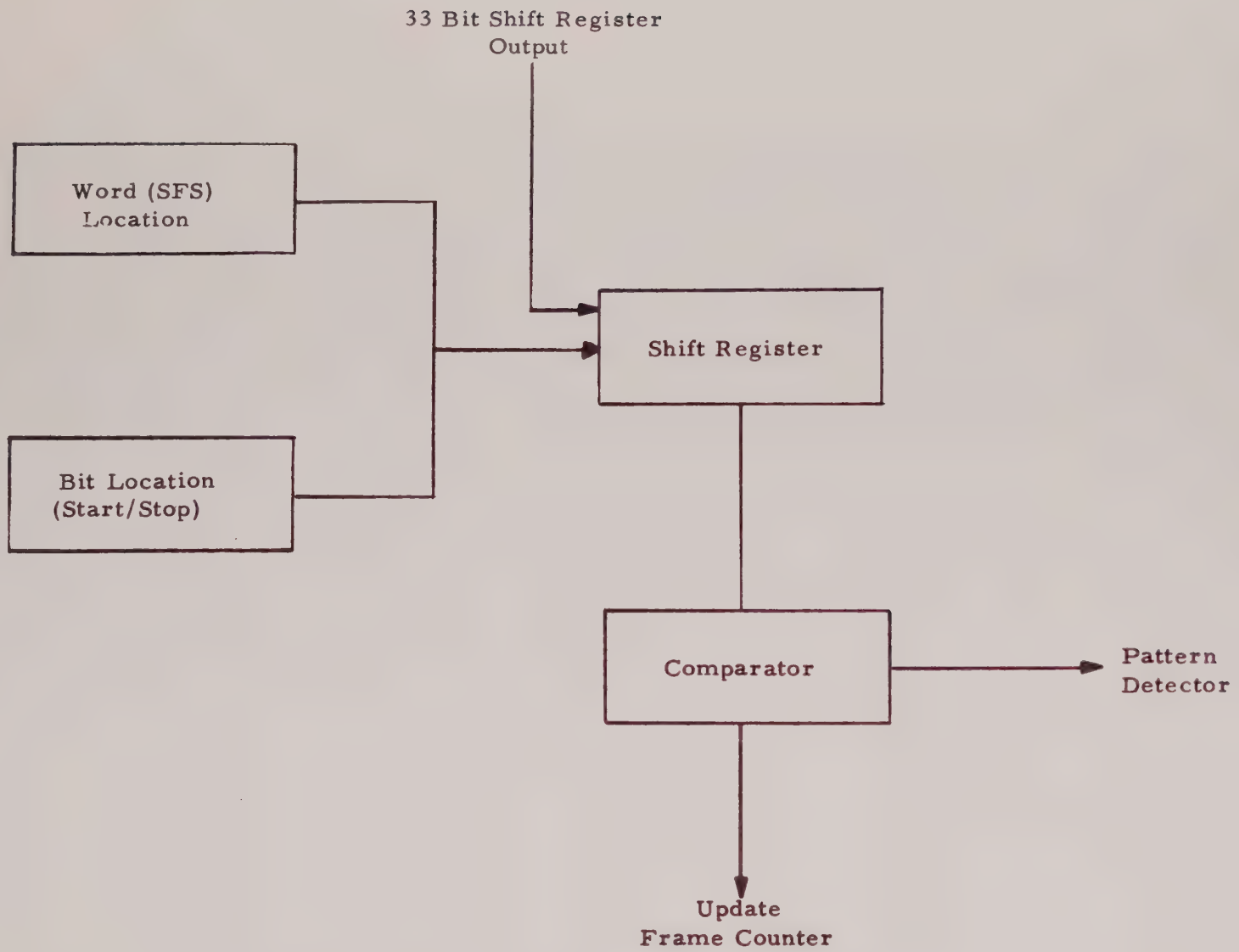


Figure 4-19. Block Diagram, SFID Synchronizer

both the frame counter and shift register contents by one count; and the comparison is made. This time agreement causes the input NAND IC12-1 and -2 to go to a high level, and causes the generation of the pattern detected (PATT DET) pulse which is applied to Correlator II.

4.6 SELECT AND MONITOR SUBSYSTEM

The select and monitor subsystem is illustrated in the block diagram of Figure 4-21. Parallel data is applied to the subsystem from the storage register of the format synchronizer section. This data is applied to the inputs of another storage register located in the select and monitor subsystem. Simultaneously, with the data; word and frame identification are applied to the word selection circuitry where any one word of the frame may be selected for display. The selected word is then strobed into storage where it remains for one frame at which time it is updated.

The output of the storage register is applied to the digital display indicators where the binary value of the selected word is displayed and to the digital to analog converter. The converted analog voltage is displayed on a voltmeter.

The output of the D/A converter is ±2.5 VDC at 5 ma which is suitable for internal system use. The amplifier shown is used to increase this capability to ±10 VDC at 100 ma making it more versatile for use in peripheral equipment.

The storage register, D/A converter and amplifier are all located on the DA/H assembly 071016, while the word selector's digital and analog displays are located on the front panel of the 4001 PCM System.

4.6.1 Digital-to-Analog Converter Assembly 071016

The parallel outputs of the storage register (of the format synchronizer section), are also applied to the rear panel of the 4001 PCM System, where they may be peripheral readout devices. These outputs are also routed to the digital-to-analog converter (D/A) assembly 071016 which contains the storage register, D/A converter and amplifier of Figure 4-21.

The schematic diagram for the D/A converter may be found in drawing 071031 and a simplified version is shown in Figure 4-22.

The 12 most significant parallel data bits from the storage register are applied to the D inputs of the flip-flops shown. Data at the inputs are changing at the word rate but are transferred to the Q side until a SELECTED WORD signal and a strobe pulse coincide to apply a pulse to the clock input of the flip-flops. The Strobe pulse, generated in the Bit Counter, is timed to arrive after the data word has had sufficient time to settle at the D inputs. The Selected Word signal is derived from the outputs of the Word Counter (which provides word identification data) and the front panel mounted SELECTED WORD switches. The SELECTED WORD goes to a high level at the appearance of the data associated with that word at the D inputs, and remains high for 1 word length.

After the data from the selected word is transferred to the buffered side of the flip-flops, the 8 most significant Q outputs are applied to transistors Q1 thru Q8 where they are converted to an analog voltage. The Q outputs are applied to the front panel mounted display lamps where they indicate the digital value of the stored data. Notice that the Q side data is updated at the selected word rate, which may be once per frame (normal), n times per frame (super-commu-

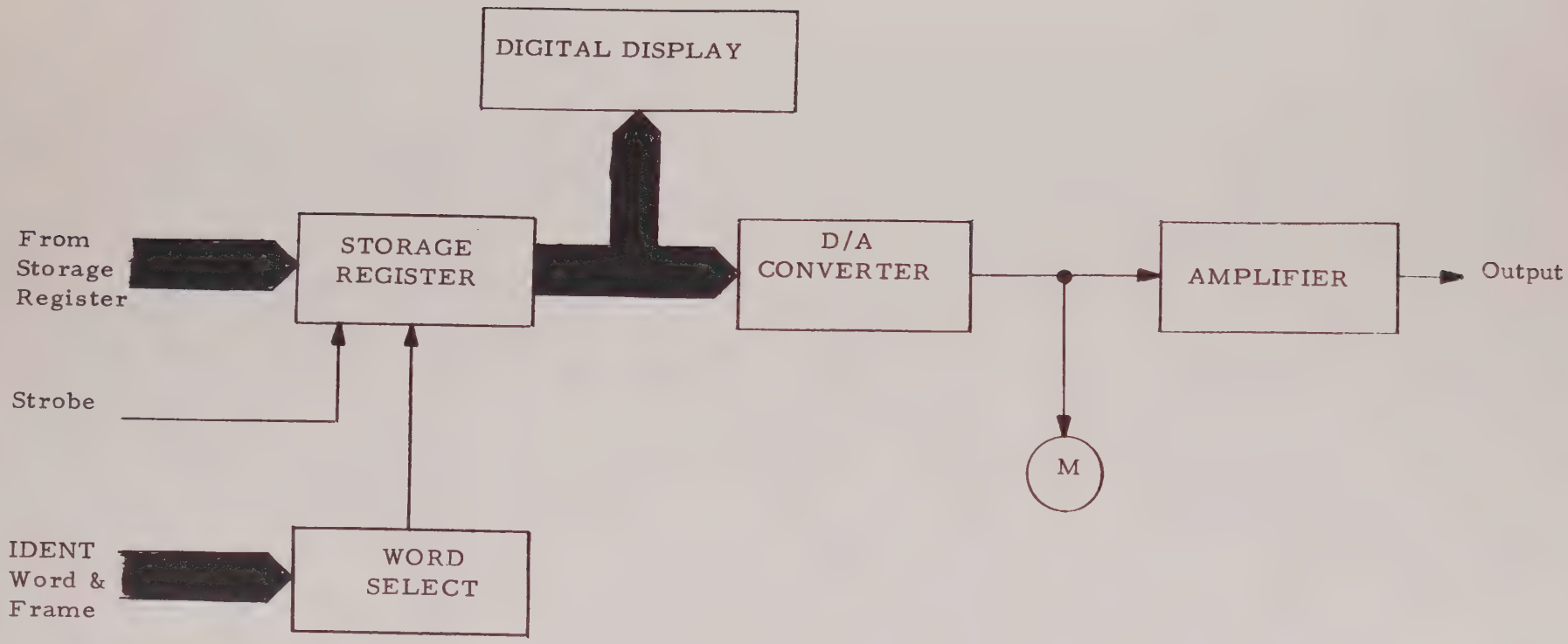
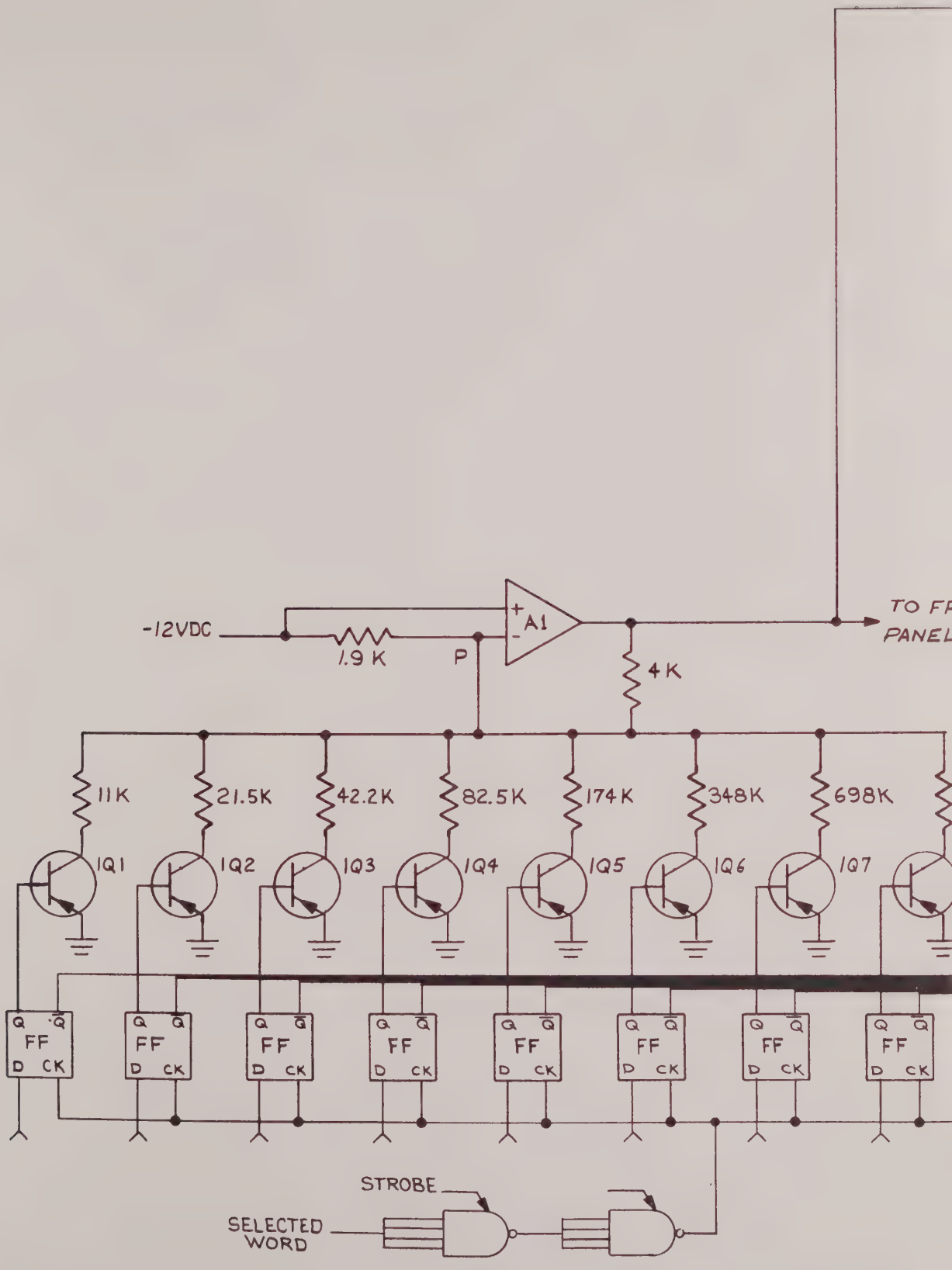
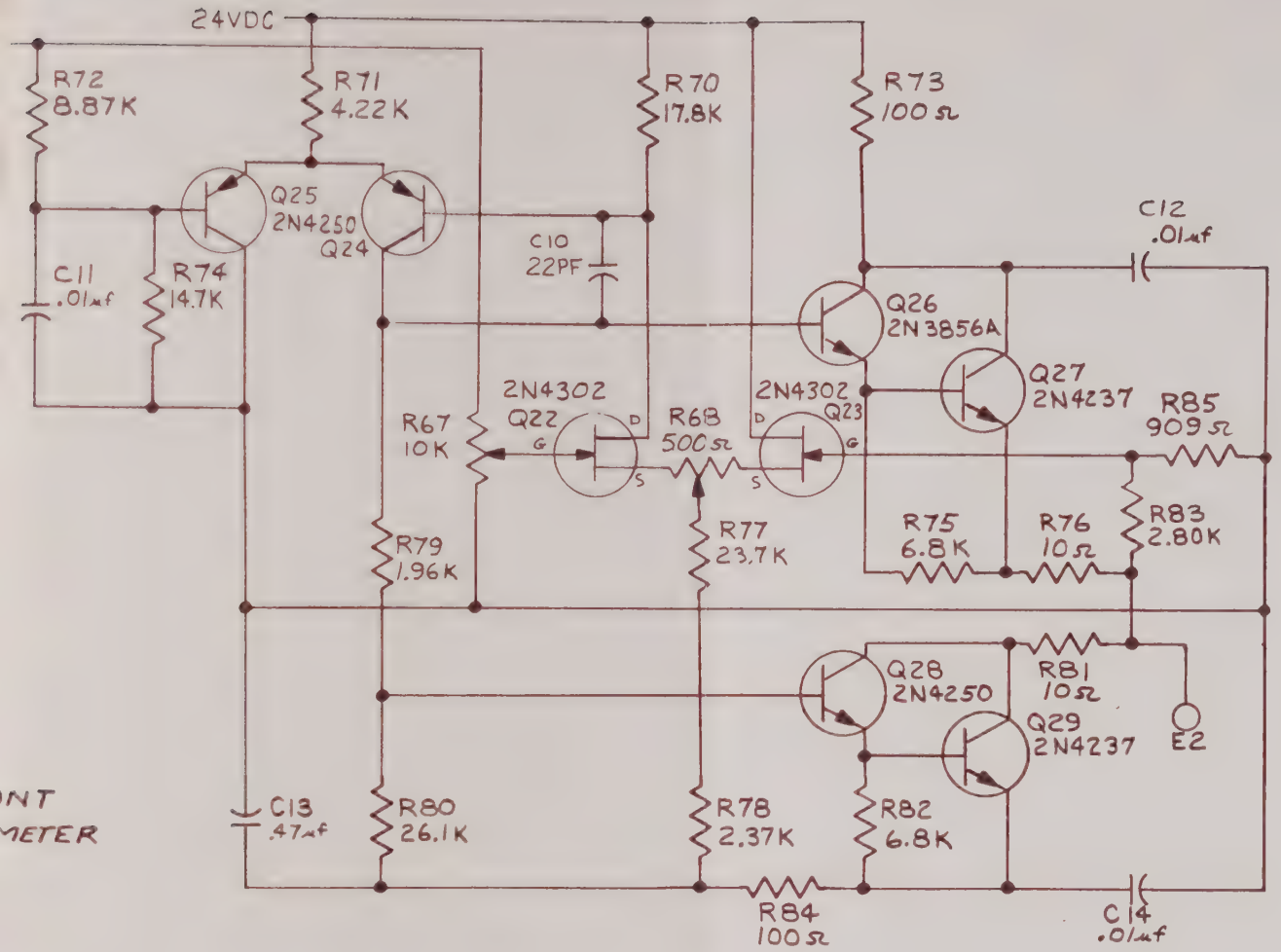


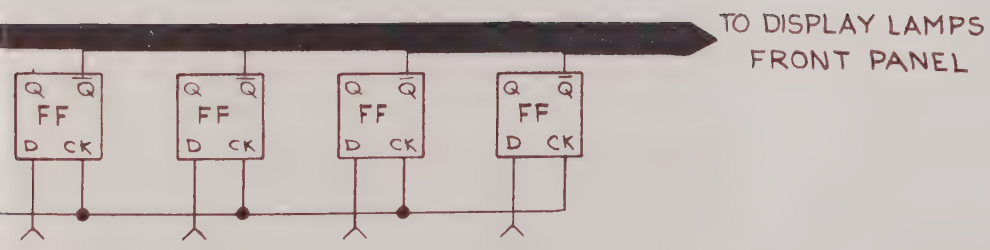
FIGURE 4-20.
Block Diagram
Select & Monitor Subsystem


-12VDC
1.9 K
P
A1
4K
TO FR
PANEL
11K
21.5K
42.2K
82.5K
174K
348K
698K
1Q1
1Q2
1Q3
1Q4
1Q5
1Q6
1Q7
Q Q
FF
D CK
STROBE
SELECTED
WORD



3 MEG.

Q8



DATA FROM PARALLEL STORAGE REGISTER

FIG. 4-21.

SIMPLIFIED SCHEMATIC
DA/H ASS'Y

tated). or once per n frame (sub-commutated). When the D/A storage register reads 00000000, the output of the differential amplifier A1 is determined by the -12 VDC supply, 1.9K and 4K input and feedback resistances, and is set at -2.5 VDC. As data is loaded into the D/A converters a logical "1" will turn on the transistor associated with the flip-flop while a logical "0" will cut it off. When any transistor is biased on, it contributes current to the node P, causing a corresponding decrease in the output. Each transistor contributes 1/2 of the current contributed by the next most significant stage. The relationship between this contribution to the output voltage is as follows:

bit	change in output voltage
2^7	2.5 VDC
2^6	1.25 VDC
2^5	.625 VDC
2^4	.3125 VDC
2^3	.15625 VDC
2^2	.078125 VDC
2^1	.0390125 VDC
2^0	.01950625 VDC

As an example, consider a data word in the register of 10110011. Upon receiving the load signal each transistor will be turned on or off depending on the previously loaded word. The analog output voltage then changes to the following:

```
-2.5
+2.5
+ .625
+ .3125
+ .03901
+ .01950
+ .99601 VDC
```

The output of amplifier A1 is applied to the analog meter located on the front panel of the system. It is also applied to the output amplifier comprised of the circuitry associated with transistors Q22 thru A29 to provide greater driving capability. The output of this amplifier

(±10 VDC) is applied to the rear connector panel where it is available for external use.

The output of the D/A converter is applied to the gate of field effect transistor (FET) Q22. Transistors Q22 and Q23 form a differential pair which provides a summing system for the input and feedback signals (thru R85 & R67), and minimizes temperature drifts and other instabilities. The drain current of Q22 is applied to the base of Q24, which with Q25 form another differential pair. Transistor Q24, in addition to, further amplifying the current, relocates the signal voltage so that it varies around ground when it is applied to the bases if Q28 and Q26. Transistors Q26, Q27, Q28, and Q29 form a two stage class B amplifier operating in push-pull. R79, R80, Q24 and the -24 VDC supply assure potentials of approximately +1.4V on the base of Q28 and -.7 V on the base of Q26 and in this manner avoid crossover distortion. As the output current of Q24 increases, emitter-followers Q26 and Q27 conduct heavily and apply the signal to the output terminals. As the collector current of Q24 decreases, Q28 and Q29 are turned on heavily since the base of Q28 is driven more negative with a decrease in Q24 collector current.

4.6.2 Word Selection

The identification information of the word and frame counters contained in the format synchronizer section is used to enable the selection of any word in the format for digital or analog display as illustrated in Figure 4-22.

Both the Q and $\overline{Q}$ outputs (ID and $\overline{ID}$) of each section of the format counters are applied to an individual thumbwheel switch as shown. These switches allow decimal selection of any word. However, notice that the individual sections of each counter is applied to the

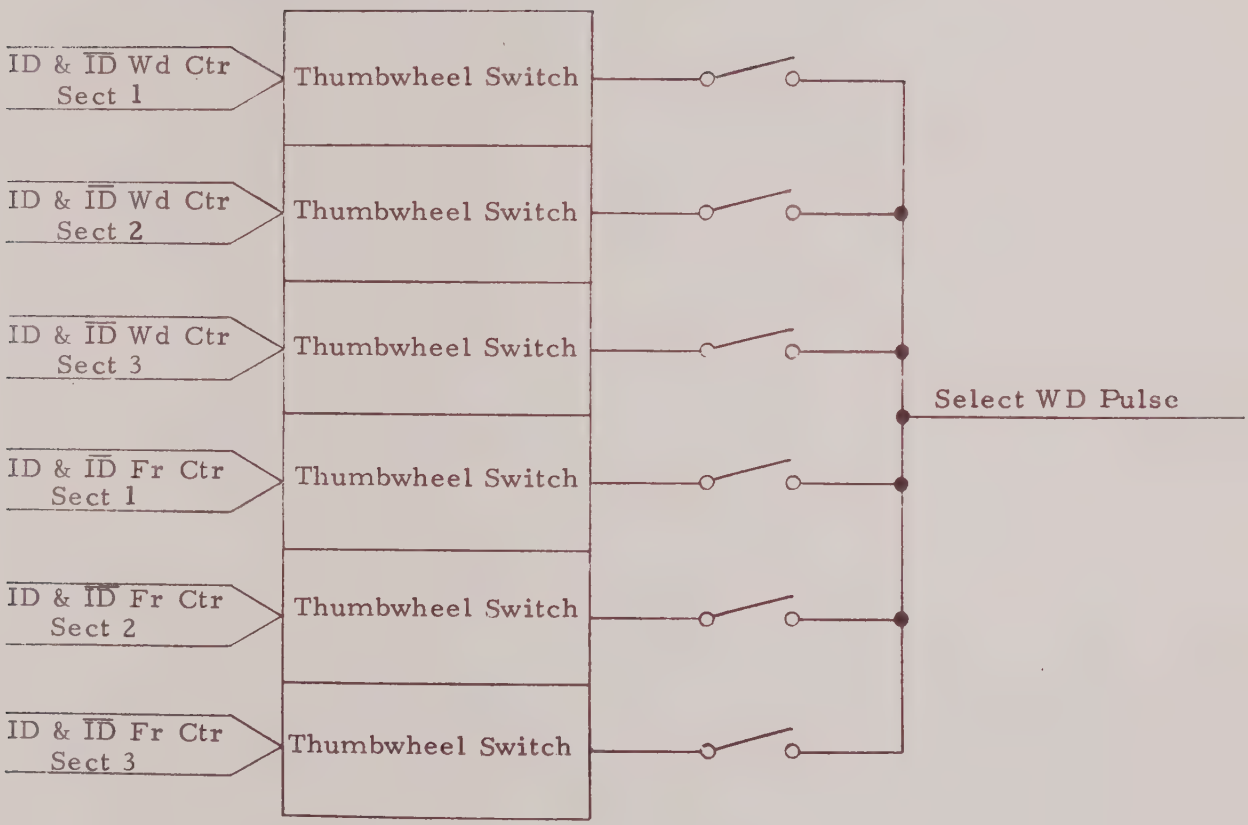

ID & $\overline{ID}$ Wd Ctr Sect 1
ID & $\overline{ID}$ Wd Ctr Sect 2
ID & $\overline{ID}$ Wd Ctr Sect 3
ID & $\overline{ID}$ Fr Ctr Sect 1
ID & $\overline{ID}$ Fr Ctr Sect 2
ID & $\overline{ID}$ Fr Ctr Sect 3
Thumbwheel Switch
Thumbwheel Switch
Thumbwheel Switch
Thumbwheel Switch
Thumbwheel Switch
Thumbwheel Switch
Select WD Pulse

Figure 4-22. Word Selector Circuit

thumbwheels separately: which allow consistent word selection regardless of the radix to which the format counters are counting. To select any word it is only necessary to dial the specific count (decimally) of each stage.

SECTION V

MAINTENANCE

5.1 GENERAL

This section provides the necessary information for the maintenance of the 4001 PCM System. Performance test, a test equipment list, component location, timing and voltage waveforms are included, (figures 5-1 through 5-3).

5.2 TEST EQUIPMENT

Table 5-1 contains a list of recommended test equipment useful in the maintenance of the 4001 PCM System.

TABLE 5-1. List of Test Equipment

Equipment Type	Manufacturer and Model
Oscilloscope	Tektronix Model 545 or equivalent
Frequency Counter	Hewlett-Packard 5532 or equivalent
Digital Voltmeter	Dymec 2401A or equivalent
Function Generator	Hewlett-Packard 202A or equivalent
Multimeter	Simpson 260 or equivalent

5.3 PREVENTIVE MAINTENANCE

Maintenance of the 4001 PCM System requires only the use of conventional hand tools normally used by the electronics technician. Periodic inspection intervals are dictated by inspection precedents established as trouble preventive measures by the using facility.

5.3.1 Visual Inspection

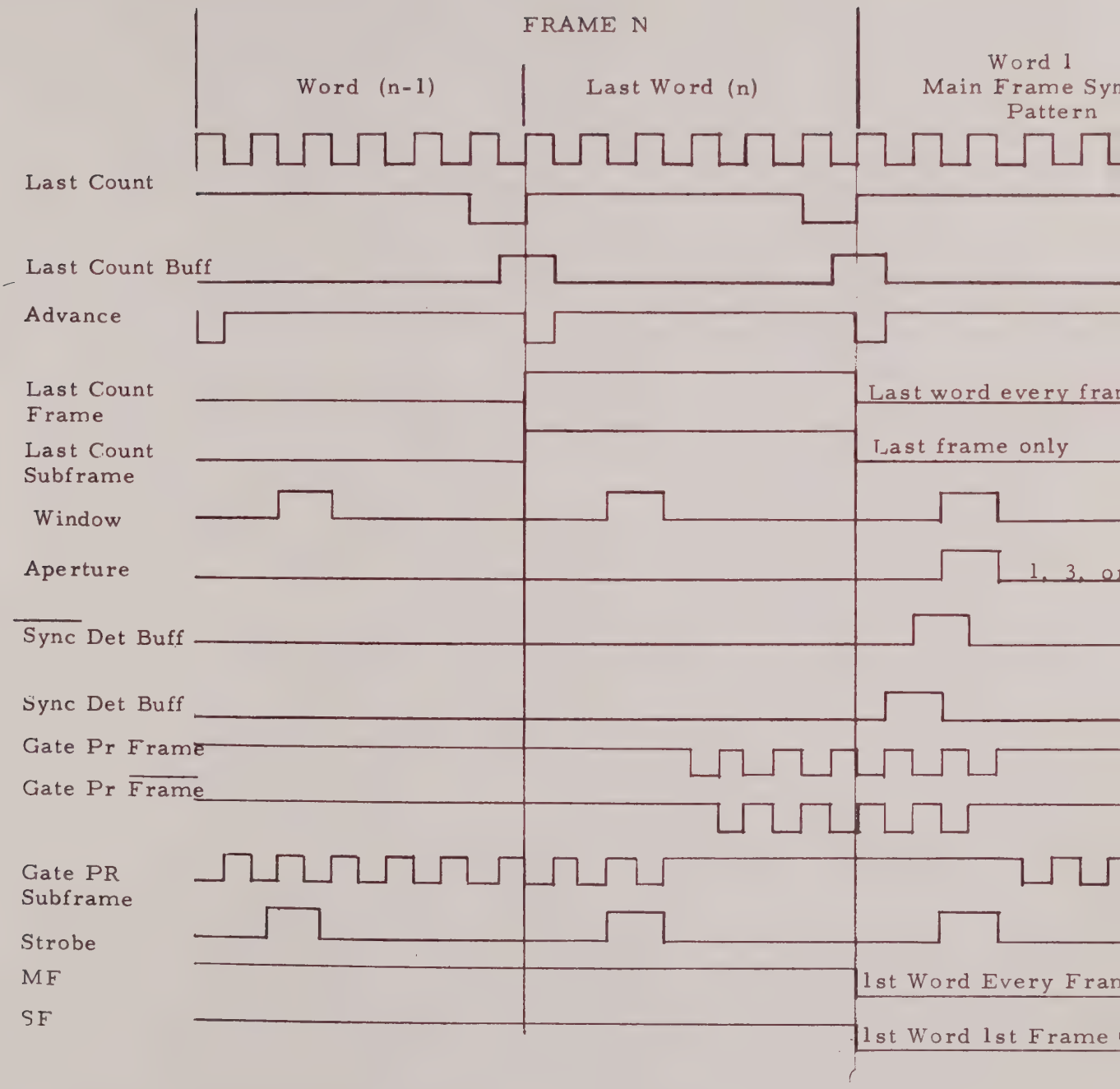
Open front and rear panels and check all circuit boards for component damage, oxidized surfaces, and burned resistors. Inspect chassis for dirt, dust, and foreign material. Remove the SBS-2 Bit Synchronizer from the 4001 PCM System. Remove the cover from the SBS-2 and perform a similar inspection.

5.3.2 Cleaning

The corners and bottom chassis of the system may be cleaned with a standard vacuum cleaner. Interior parts to the bit synchronizer and all board assemblies should be cleaned with an air jet (25 psi or less). The front panels may be cleaned with carbon tetrachloride or any equivalent solvent.

5.3.3 Lubrication

To ensure continued reliable operation of the system, all fans should be lubricated at least every six months or less depending


FRAME N
Word (n-1)
Last Word (n)
Word 1
Main Frame Syn
Pattern
Last Count
Last Count Buff
Advance
Last Count
Frame
Last word every fra
Last Count
Subframe
Last frame only
Window
Aperture
1, 3, o
Sync Det Buff
Sync Det Buff
Gate Pr Frame
Gate Pr Frame
Gate PR
Subframe
Strobe
MF
1st Word Every Fra
SF
1st Word 1st Frame

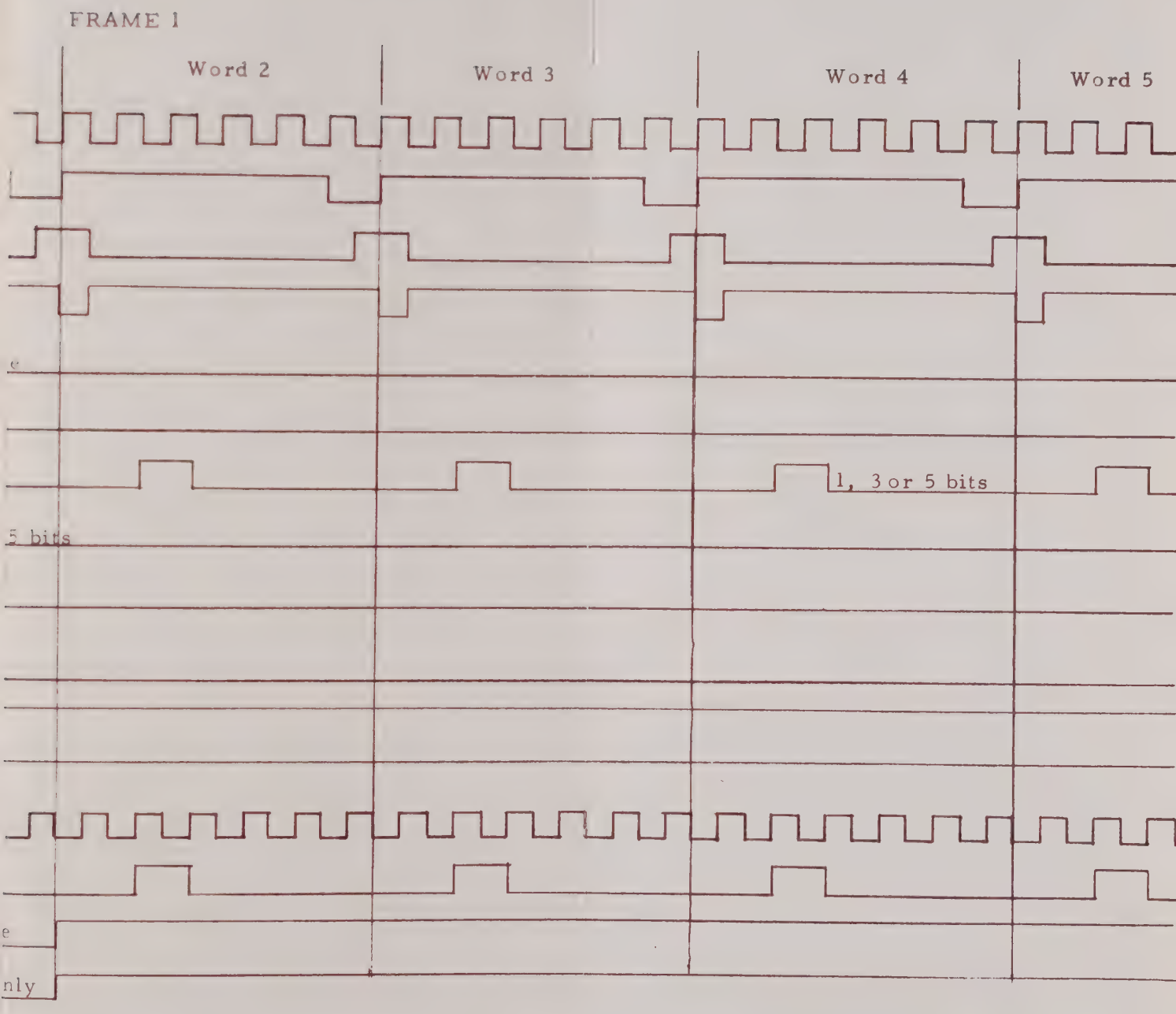
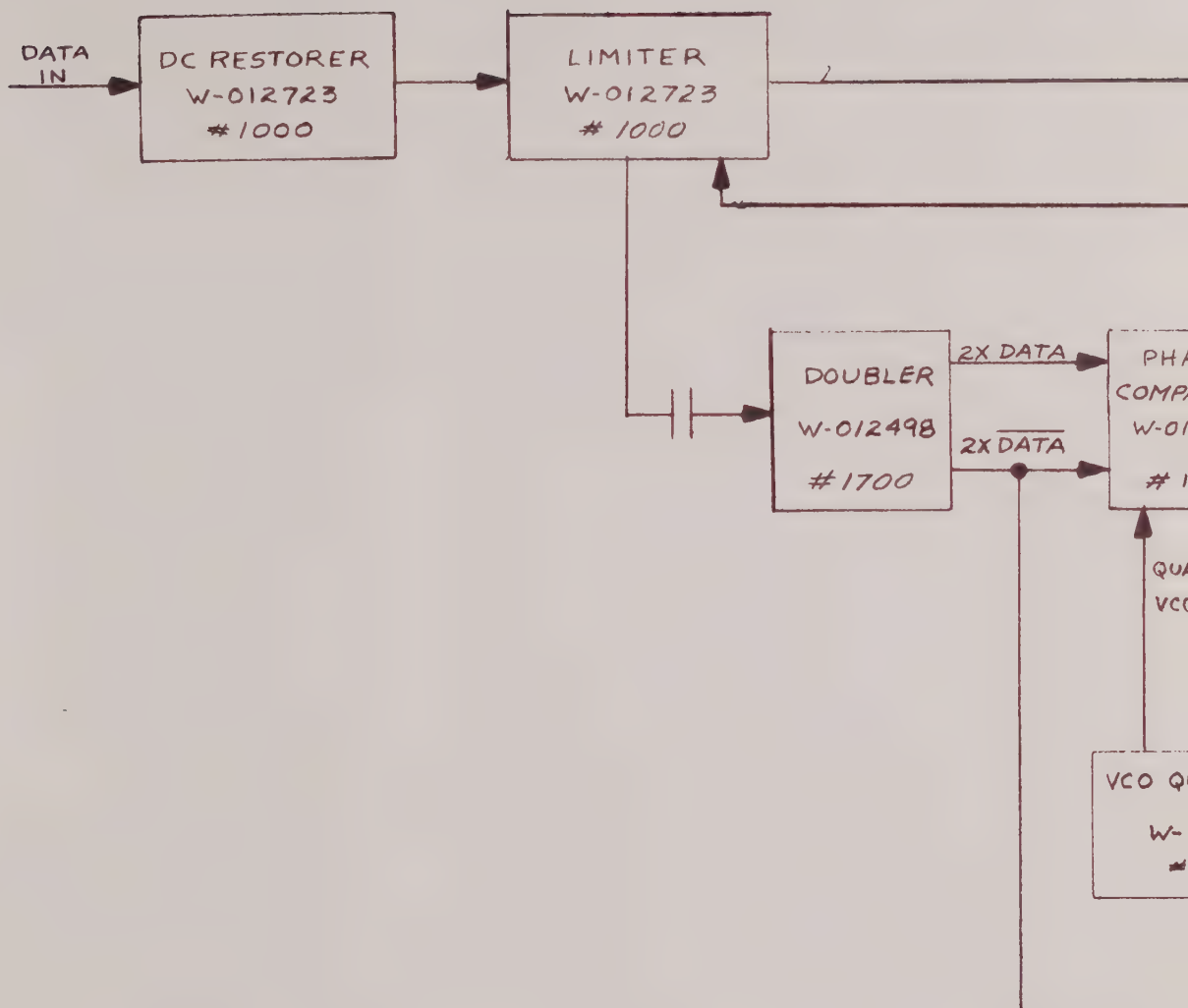


FIGURE 5-1.

Timing Diagram
Major Pulses
4001 PCM System
Format Sync Section


DATA IN
DC RESTORER
W-012723
#1000
LIMITER
W-012723
#1000
DOUBLER
W-012498
#1700
2X DATA
2X $\overline{\text{DATA}}$
METER BD.
W-012514
#3400

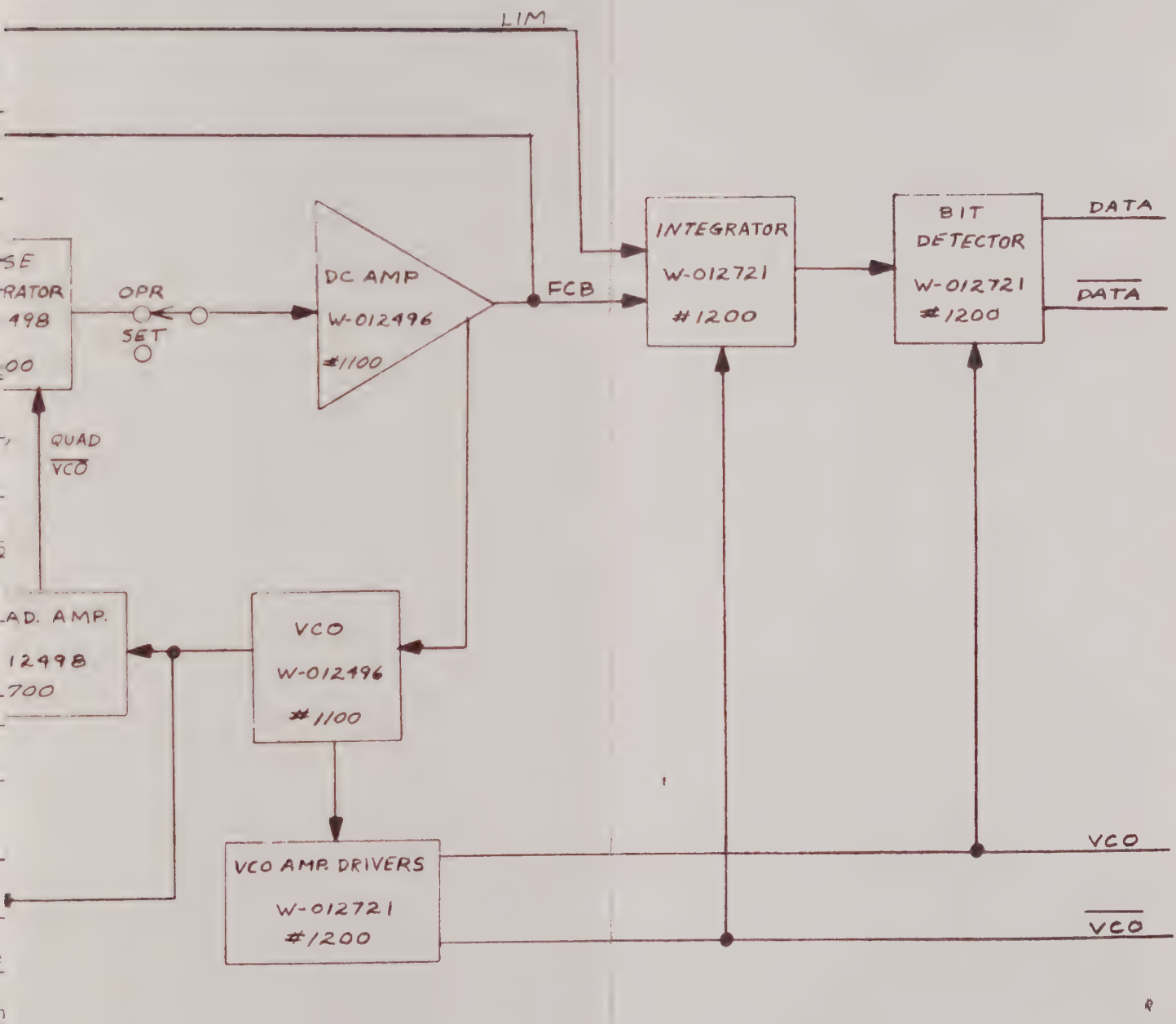
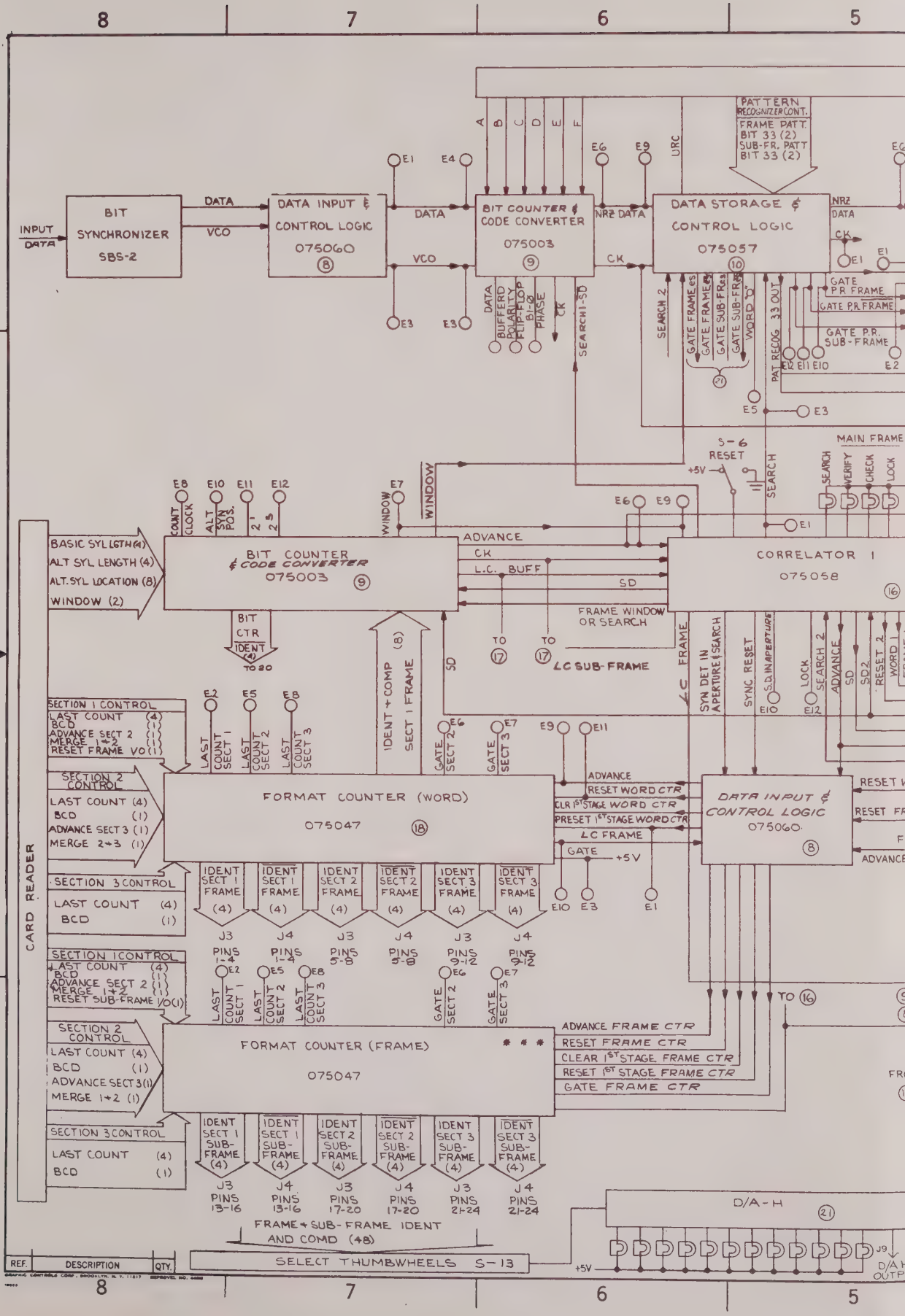


Figure 5-2. Maintenance Block Diagram, SBS-2 Bit Synchronizer


BIT SYNCHRONIZER SBS-2
INPUT DATA
DATA
VCO
DATA INPUT & CONTROL LOGIC 075060 (8)
BIT COUNTER & CODE CONVERTER 075003 (9)
DATA STORAGE & CONTROL LOGIC 075057 (10)
PATTERN RECOGNIZER CONT.
FRAME PATT. BIT 33 (2)
SUB-FR. PATT BIT 33 (2)
NRZ DATA
CK
URC
GATE P.R. FRAME
GATE P.R. SUB-FRAME
PAT RECOG 33 OUT
S-6 RESET
+5V
SEARCH
VERIFY
CHECK
LOCK
MAIN FRAME
BASIC SYL LGTH (4)
ALT SYL LENGTH (4)
ALT. SYL LOCATION (8)
WINDOW (2)
BIT COUNTER & CODE CONVERTER 075003 (9)
ADVANCE
L.C. BUFF
SD
CORRELATOR I 075058 (16)
FRAME WINDOW OR SEARCH
LC SUB-FRAME
SYN DET IN APERTURE
SYNC RESET
LOCK
SEARCH 2
RESET 2
BIT CTR IDENT (4) TO 20
IDENT + COMP (8) SECT 1 FRAME
SECTION 1 CONTROL
LAST COUNT (4) BCD
ADVANCE SECT 2
MERGE 1+2 (1)
RESET FRAME VO (1)
SECTION 2 CONTROL
LAST COUNT (4) BCD (1)
ADVANCE SECT 3 (1)
MERGE 2+3 (1)
SECTION 3 CONTROL
LAST COUNT (4) BCD (1)
SECTION 1 CONTROL
LAST COUNT (4) BCD
ADVANCE SECT 2
MERGE 1+2
RESET SUB-FRAME VO (1)
SECTION 2 CONTROL
LAST COUNT (4)
BCD (1)
ADVANCE SECT 3 (1)
MERGE 1+2 (1)
SECTION 3 CONTROL
LAST COUNT (4) BCD (1)
CARD READER
FORMAT COUNTER (WORD) 075047 (18)
FORMAT COUNTER (FRAME) 075047
DATA INPUT & CONTROL LOGIC 075060 (8)
ADVANCE
RESET WORD CTR
CLR 1ST STAGE WORD CTR
PRESET 1ST STAGE WORD CTR
LC FRAME
GATE
+5V
IDENT SECT 1 FRAME (4)
IDENT SECT 2 FRAME (4)
IDENT SECT 3 FRAME (4)
J3 PINS 1-4
J4 PINS 1-4
J3 PINS 5-8
J4 PINS 5-8
J3 PINS 9-12
J4 PINS 9-12
ADVANCE FRAME CTR
RESET FRAME CTR
CLEAR 1ST STAGE FRAME CTR
RESET 1ST STAGE FRAME CTR
GATE FRAME CTR
IDENT SECT 1 SUB-FRAME (4)
IDENT SECT 2 SUB-FRAME (4)
IDENT SECT 3 SUB-FRAME (4)
J3 PINS 13-16
J4 PINS 13-16
J3 PINS 17-20
J4 PINS 17-20
J3 PINS 21-24
J4 PINS 21-24
FRAME + SUB-FRAME IDENT AND COMD (48)
SELECT THUMBWHEELS S-13
D/A-H (21)
REF. DESCRIPTION QTY.

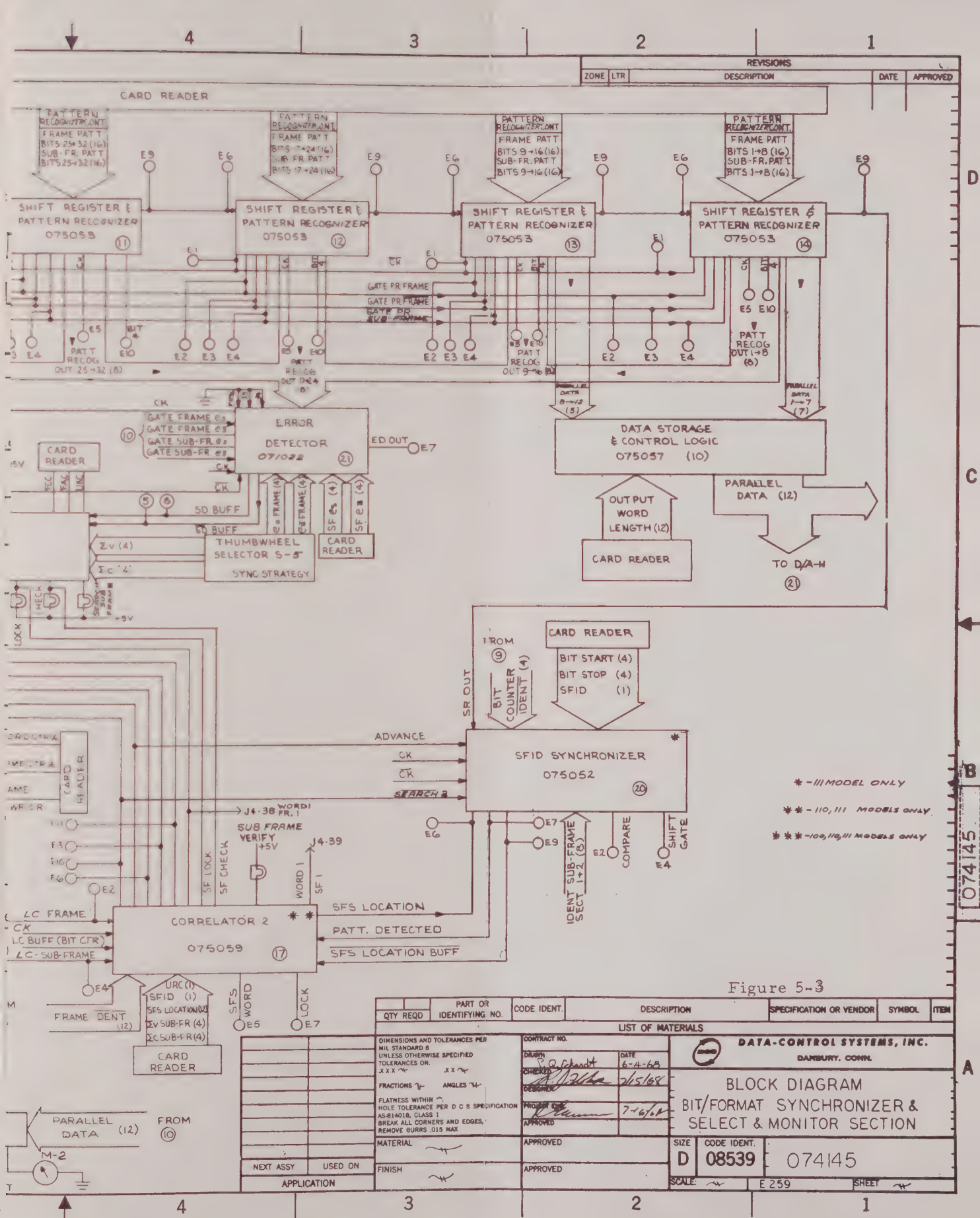


Figure 5-3

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8 UNLESS OTHERWISE SPECIFIED TOLERANCES ON. XXX ± XX ± FRACTIONS ± ANGLES ± FLATNESS WITHIN HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1 BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

CONTRACT NO.

DRAWN Q. Schandt DATE 6-4-68

CHECKED 7/5/68

DESIGNED

PROJECT ENG. 7-16-68

APPROVED

APPROVED

APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BLOCK DIAGRAM BIT/FORMAT SYNCHRONIZER & SELECT & MONITOR SECTION

SIZE D | CODE IDENT. 08539 | 074145

SCALE: | E 259 | SHEET

074145

on system useage. General purpose light weight lubricating oil should be used as follows:

a) Load hypodermic needle with approximately 10cc of oil,

b) Place the needle at the center of the circle marked on the Gold label of the fan at an angle of approximately 45^{o}

c) Pierce the label and concealed self-sealing rubber cap located under the label,

d) Insert the needle approximately 1/4" and discharge the oil.

5.3.4 Periodic Inspections and Adjustments

The following inspections and adjustments (if necessary) should be made during preventive maintenance down time.

5.3.4.1 SBS-2 Bit Synchronizer - DC Balance Adjustment

In order to adjust the balance of the DC restorer and limiter assembly proceed as follows:

a. Open the front panel door of the system and remove the side cover from the SBS-2 Bit Synchronizer. Place the synchronizer on an extender and reinstall. On the front panel (bit synchronizer section) set:

NOR/INV switch to NOR
WIDE/NAR switch to WIDE
OPR/SET switch to OPR

b. Monitor test point (TP) 1001 of the DC restorer and limiter assembly, TA-011756, with a digital voltmeter (DC), and place a short circuit at rear panel connector J5. Adjust R1016 on the DC restorer and limiter for zero volts on the DVM.

c. Connect the output of the function generator (sine) to J5. Set the frequency to 1/2 the mean value of the bit rate range of the tuning unit installed,and set the amplitude to some convenient value between 0.5 and 25 volts peak-to-peak.

d. Monitor TP1702 with the oscilloscope and adjust the display to obtain 1 full period across the face of the scope.

e. Adjust potentiometer R1039 (on the DC restorer and limiter assembly) to obtain a 50% duty cycle.

5.3.4.2 SBS-2 Bit Synchronizer - Phase-Lock-Loop Adjustment

The adjustment of the phase-lock-loop circuitry in the SBS-2 circuitry is accomplished as follows:

a. Connect a frequency counter to the VCO monitor jack on the front panel of the system and adjust the ADJ FREQ potentiometer for a frequency equivalent to the mean of the bit rate range of the tuning unit installed.

b. Place the DC voltmeter to TP1701, place the OPR/SET switch to SET and adjust potentiometer R1139 to obtain 0 volts on the voltmeter.

c. Place a short circuit at rear panel connector J5, turn the OPR/SET switch to OPR and adjust potentiometer R1149 for zero volts on the meter.

d. Connect a frequency counter to the junction of CR1107 and R1125 (on the extreme right of the circuit board) and adjust R1105 until a frequency equivalent to twice the mean value of the bit rate range is obtained.

e. Place J8 to the vertical input of the oscilloscope and display one full wave as in step (d) of 5.4.3.1 and adjust R1115 for 50% duty cycle.

5.3.4.3 SBS-2 Bit Synchronizer - Meter Circuit Adjustment

The meter circuit is balanced as follows:

a. Turn the OPR/SET switch to SET and monitor TP3401 with the oscilloscope.

b. Display one full wave on the oscilloscope as in step (d) of 5.4.3.1 and adjust R3401 for a 50% duty cycle.

5.3.4.4 SBS-2 Bit Synchronizer - Quadrature VCO Symmetry Alignment

The alignment of the quadrature VCO circuits is accomplished as follows:

a. Place the OPR/SET switch to OPR and connect the DVM to TP1701. Adjust the potentiometer R1139 for 0 volts.

b. Set the noise generator range to RF and adjust the output amplitude for 2 V RMS. Apply the generator output to J5.

c. Adjust potentiometer R1735 for 0 ±.3 volts.

5.3.4.5 Format Synchronizer - Power Supply

The power supply is adjusted as follows:

a. Open the rear panel door and apply a DC voltmeter to the +24 VDC terminals on the power supply and adjust to +24 VDC ±.5 VDC. Repeat for the -24 VDC supply.

b. Apply the voltmeter to the +5 VDC terminals and adjust the 5V adjustment potentiometer for 5.00 VDC +0 - .25 VDC.

5.4 CORRECTIVE MAINTENANCE

5.4.1 Circuit Location

All circuits used in the Model 4001 PCM System are contained on printed circuit boards mounted in numbered card guides located directly behind the front panel. Table 5-2 correlates card numbers to card types.

5.4.1.1 SBS-2 Bit Synchronizer Circuit Location

The SBS-2 Bit Synchronizer located in card files 1 thru 7 is a modularized subsystem containing the following circuit board assemblies:

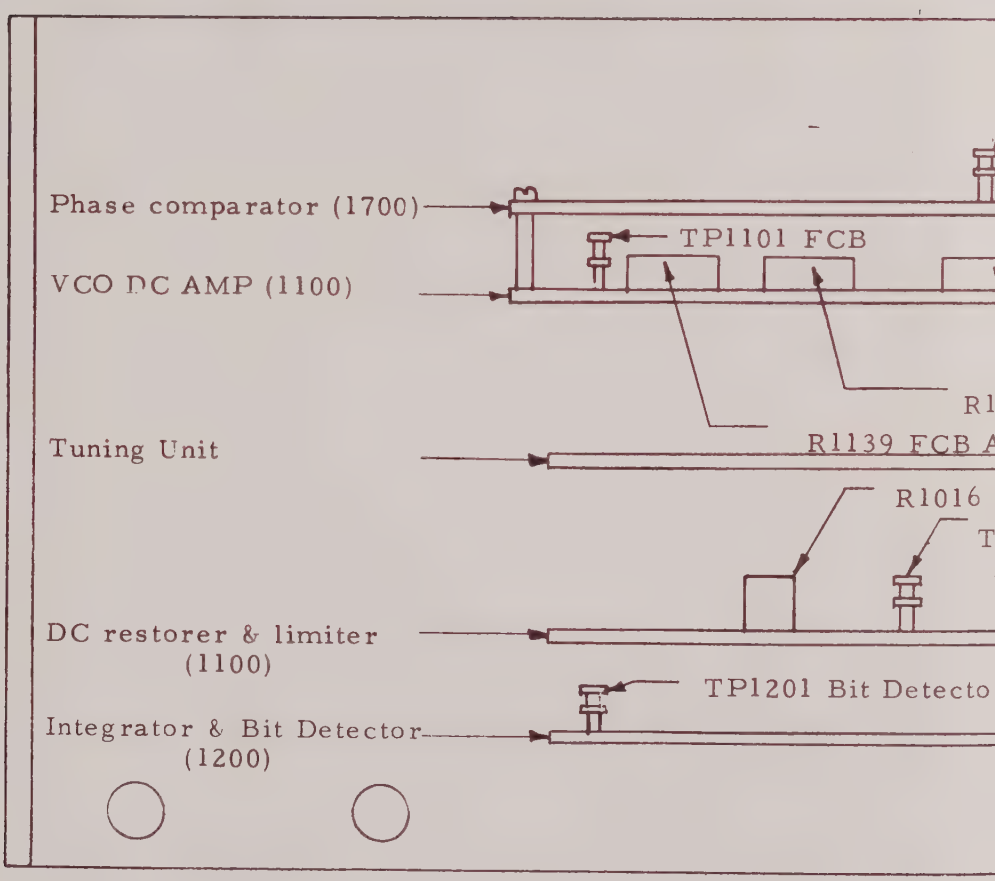
Designator	P/N	Nomenclature
1700	12105	Phase Comparator Assembly
1100	11734	VCO DC Amplifier Assembly
	84448	Heatsink Assembly
3400	11157	Meter Board Assembly
		Tuning Unit Assembly
1000	11756	DC Restorer and Limiter
1200	11577	Integrator and Bit Detector
200	11460	+8, +12V Power Supply Assembly
100	11471	-4, -8, -12V Power Supply Assembly

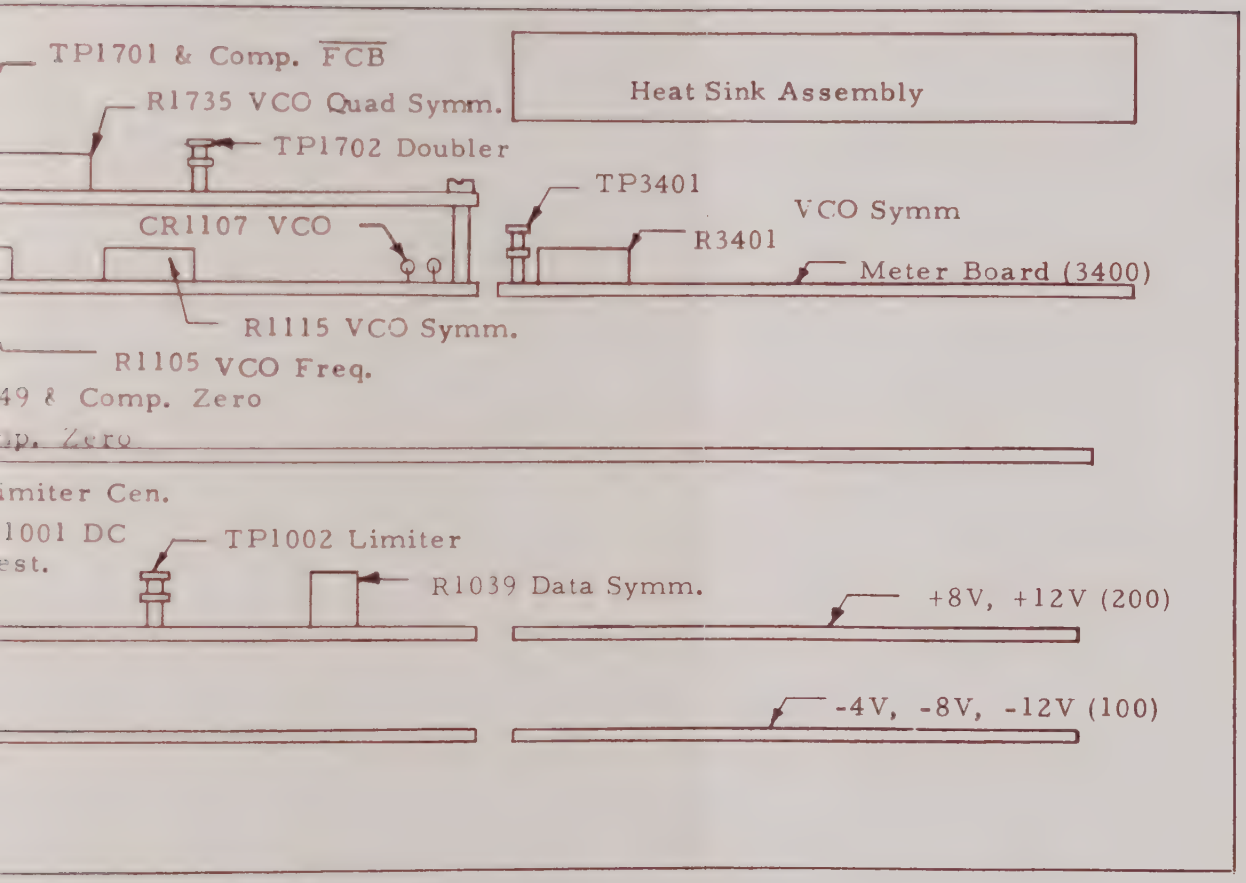
The designator shown in the first column is an arbitrary number assigned to each board assembly in order to facilitate component location. The locations of these circuit board assemblies are shown in Figure 5-4.

Table 5-2. Circuit Location 4001 PCM System

Card File No.	Circuit Ass'y. No.	Nomenclature
1	SBS-2	Bit Synchronizer Assembly
2	SBS-2	Bit Synchronizer Assembly
3	SBS-2	Bit Synchronizer Assembly
4	SBS-2	Bit Synchronizer Assembly
5	SBS-2	Bit Synchronizer Assembly
6	SBS-2	Bit Synchronizer Assembly
7	SBS-2	Bit Synchronizer Assembly
8	070060	Data Input & Control Assembly
9	070003	Code Converter & Bit Counter Ass'y.
10	070057	Data Storage & Control Assembly
11	070053	Shift Register & Pattern Recognizer Assembly
12	070053	Shift Register & Pattern Recognizer Assembly
13	070053	Shift Register & Pattern Recognizer Assembly
14	070053	Shift Register & Pattern Recognizer Assembly
15	071022	Error Detector Assembly
16	070058	Correlator Assembly
17	*070059	Correlator II Assembly
18	070047	Format Counter Assembly (Word)
19	**070047	Format Counter Assembly (Frame)
20	***070052	SFID Synchronizer Assembly
21	071016	D/A Converter Assembly

*Models -111 & -110 only
**Models -111, -110, and -100 only
***Model -111 only


Phase comparator (1700)
TP1101 FCB
VCO DC AMP (1100)
R1
Tuning Unit
R1139 FCB A
R1016
T
DC restorer & limiter
(1100)
TP1201 Bit Detecto
Integrator & Bit Detector
(1200)



SBS-2 BIT SYNCHRONIZER
CARD LAYOUT

Figure 5-4.

5.4.2 COMPONENT LOCATION

There are two basic circuit configuration types used in the 4001 PCM System: a DCS configuration known as "Auto-Board", and the commonly encountered discrete component board. The "Auto-Board", so called because of the automatic manufacturing processes used, is the standard configuration for all DCS logic. Component designators on all auto boards are coded to give location as well as integrated circuit identification. The key is given in Figure 5-5. An "Auto-Board" is identifiable by the presence of 070 in the first 3 digits of its assembly number.

Component locations for the discrete component boards contained in the 4001 PCM System may be found on the applicable assembly print in Section VIII.

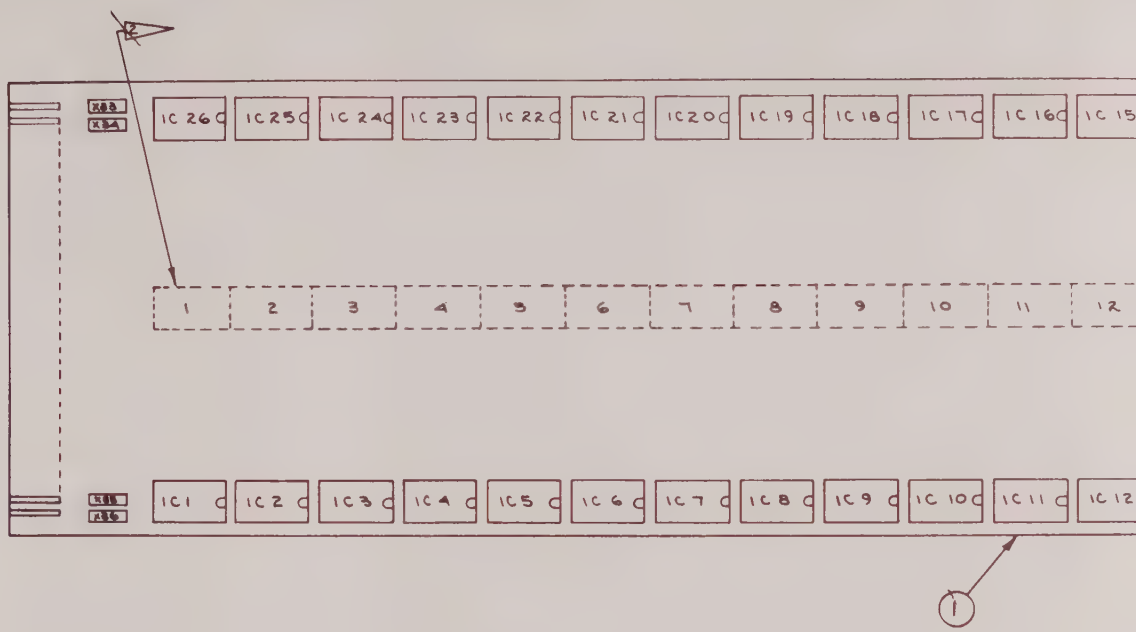
5.4.3 Trouble-Shooting

Since the bit synchronizer section is basically an analog device, the trouble-shooting by localization to a subsystem, then to a circuit board, and finally to a component, is recommended. However, because of the complex timing relation ships and feedback paths, this approach is not recommended for the localization of malfunctions in the digital circuits of the 4001 PCM system. When trouble occurs the suspicious circuit should be investigated throughout the system rather than striving to isolate the fault by testing any circuit board out completely prior to moving on to the next, with the aid of the timing and block diagrams of figures 5-1 thru 5-3.

Generally, all digital pulses will be a nominal 4 volts and rise time are usually between 20 and 40 nanoseconds. All pulses greatly exceeding these ranges should be checked.

5.4.4 Component Removal

Because of the narrow lands used on the auto boards, special care must be exercised when removing Integrated Circuits from the boards. The wicking method of chip removal is



IC POS. CHART	
IC 1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
IC 26	

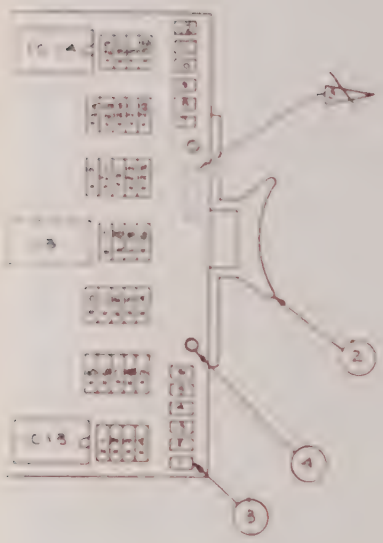
COMP POS. CHART	
X1	
X2	
X3	
X4	
X5	
X6	
X7	
X8	
X9	
X10	
X11	
X12	
X13	
X14	
X15	
X16	
X17	
X18	
X19	
X20	
X21	
X22	
X23	
X24	
X25	
X26	
X27	
X28	
X29	
X30	
X31	
X32	
4 X33	JUMP
X34	.1UF 25V
X35	.1UF 25V
4 X36	JUMP

NOTES:

1. DRILL MATRIX HO
2. REPAIR PAD SE
3. STAMP ASSEMBL SHOWN USING WHI
4. USE #22 AWG S
5. FOR LOGIC SE
6. SEE IC POSITIO
7. SEE COMP. POS
8. INSTALL ITEM

REF.	DESCRIPTION	QTY.
A	.014 DIA #79 DR.	AR 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ES PER PAPER PUNCH TAPE #070 REV
TIONS 1-15
NO IN 3/32 HIGH CHARACTERS APPROX. AS
E INDELIBLE INK.
LID WIRE.
075
CHART.
ION CHART.
IN 'A' HOLES.

ITEM	SYMBOL	SPECIFICATION OR VENDOR	DESCRIPTION	CODE IDENT.	PART OR IDENTIFYING NO.	QTY REQD
6			CONNECTION PIN		016467	A/R
5		6PRAGUE	CAPACITOR .1UF 25V		3C023	2
4		CTC	RIVET		1200-5-02	2
8		AUGAT	TEST JACK		8046-1	12
2		8STANFORD APPLIED	CARD PULL		SAE 6200	1
1			BOARD SUB-ASSY		079009	1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
XXX — XX —
FRACTIONS — ANGLES —
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION

CONTRACT NO.
DRAWN | DATE
CHECKED
ENGINEER
PROJECT ENG.
APPROVED
APPROVED
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y
AUTO-BOARD

SIZE D | CODE IDENT. 08539 | FIGURE 5-5.
SCALE: — | SHEET —

recommended and is accomplished as follows:

a) Strip approximately 1/2" of insulation from a piece of stranded wire (19 strand is preferable) and with a pair of pliers flatten the exposed end.

b) Dip the flattened end in liquid flux

c) Place the fluxed wire on the solder connection(s) and place the tip of the soldering iron on the wire

d) Remove the tip and wire simultaneously as soon as the solder has wicked on to the wire.

5.5 PERFORMANCE TEST PROCEDURES

To checkout the performance of the 4001 PCM System to the fullest extent of its capability would necessitate a time expenditure far out of proportion to normal checkout or calibration procedures. An appreciation of the complexity of these tests is obtained when considering the word and frame counters in the format synchronizer section. Each counter is a 12-stage parallel counter which may count to 4096, be programmed to reset at any of these counts, and may be configured to count to any radix.

Since the 4001 PCM System does not include a simulator, the performance of the System is evaluated by applying PCM data of a known format to connector J5 and monitoring the serial PCM wavetrain at connector J7 for the correct NR2-L data output. Select a specific word with the SELECTED CHANNEL switches and verify that the selected word is displayed on the digital display lamps and the analog meter located on the select and monitor front panel.

SECTION VI

GLOSSARY

6.1 The glossary given on the following pages is presented to define non-standard PCM terms used in this instruction manual.

6.1.1 FORMAT TERMS

FAC: Frame Alternating Complement - A synchronization pattern which is complemented on alternate frames. A FAC sync pattern is used to provide additional confidence in the main frame synchronization.

FCC: Frame Code Complement - A synchronization pattern which is complemented for one frame at the subframe rate.

Bit: A Binary Digit. The smallest unit of information in the PCM System.

Bit Time: The period of a bit. In this instruction manual one bit time is equivalent to one clock cycle.

Channel: A specific position of a commutator.

Format: The parameters of a PCM code which describe and define it.

Frame (Main): A series of words encompassing all positions of a commutator. To avoid confusion with a subframe, the frame is sometimes referred to as the main frame. Note that as used in this instruction manual, the main frame does not include all subcommutated channels.

Subframe: A series of words located in a specific channel(s) of the main frame and which are commutated at a slower rate than main frame words.

Alt. Syliable: Part of a word used in formats containing variable word lengths.

Unique Recycling Code (URC): A subframe synchronization patterns which is inserted in the data once per subframe to indicate the first subframe. The URC differs from the Frame Code Complement in that it may appear in any word of the frame.

Word: A coded series of bits which represent a channel value during one sample time.

Word Length: Number of bits per word.

6.1.2 GENERAL TERMS

Binary Coded Variable Radix (BCVR): A configuration of the word and frame counters which will count to a base other than two.

6.1.3 MAJOR CONTROL SIGNALS

ADVANCE (ADV): The ADVANCE pulse is generated in the bit counter and is used to trigger the word and frame counters as well as other control circuits in the 4002 PCM System. ADVANCE is a normally high level which goes low on the first clock of every word and rises on $\overline{\text{CLOCK}}$. Duration - 1/2 clock cycle.

APERTURE: The APERTURE is a normally low level which rises at the specific bit time at which a synchronization pattern is expected to be detected by the pattern recognizer. The relative occurrence of the APERTURE and SYNC DETECTED pulse provide the foundation upon which the synchronization of the PCM System is evaluated. Duration - 1, 3, or 5 bits depending on the window duration.

GATE PR FRAME:	This signal is used to gate the bit recognizers when looking for the frame sync pattern.
GATE PR $\overline{\text{FRAME}}$:	This signal is used to gate the bit recognizers when looking for the complementary sync pattern.
GATE PR SUB-FRAME:	This signal is used to gate the pattern recognizer when looking for a URC sync pattern.
MF:	Main Frame - This signal is available on the front panel of the PCM System where it may be used for general purpose synchronization. Normally a high level, the MF goes low on the first word of every frame. Duration - 1 word.
LAST COUNT (LC):	A control signal generated in the bit counter. LAST COUNT is a normally high level signal which goes low for the last bit of each word or syllable and rises again on the first clock of the next word. Duration - 1 clock cycle.
LAST COUNT FRAME (LCF):	The LAST COUNT FRAME is normally a low level which rises on the first bit of the last word of every frame and falls on the first bit of the following word. The LCF indicates that the last word of the frame is being counted in the word counter. Duration - 1 word.
LAST COUNT SUBFRAME (LCSF):	The LAST COUNT SUBFRAME is normally a low level which rises on the first bit of the last word of the last frame of the format. Duration - 1 word.

SF:	Subframe - This signal is available on the front panel of the PCM System where it may be used for general purpose synchronization. Normally a high level the SF goes low on the first word of the first frame of the data cycle. Duration - 1 word.
STROBE:	The STROBE is used in the Select and Monitor section and in peripheral equipment to load a data word into storage or digital-to-analog converters. The STROBE appears at word rate and is timed to occur after the data word has had sufficient time to settle in storage. Duration - 1 clock cycle.
SYNCHRONIZATION PATTERN DETECTED (SYNC DET):	This signal is normally a low level. When the pattern recognizer has detected a sync pattern, this pulse goes high for 1 clock cycle. The relative occurrence of the SYNC DET pulse and the APERTURE provides the foundation upon which the synchronization of the PCM System is evaluated. Duration - 1 clock cycle.
WINDOW:	The WINDOW is a normally low level which rises for 1, 3 or 5 bits every word. The window represents the bit position(s) in every word when a synchronization pattern may be detected. The WINDOW in conjunction with LAST COUNT FRAME is used to generate the APERTURE.

REAR VIEW OF CIRCUT BOARD

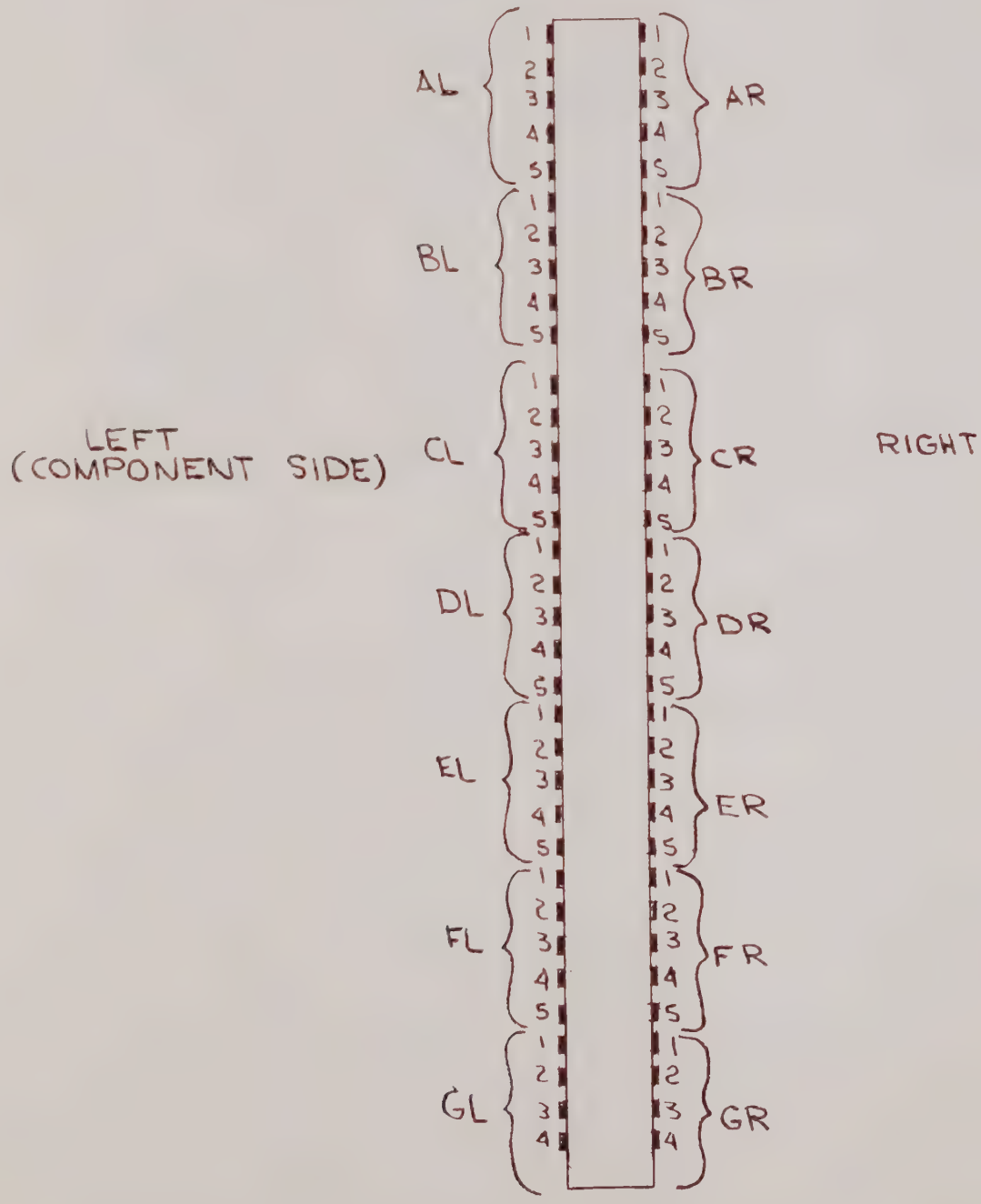


FIGURE 7-1 CIRCUT BOARD CONNECTOR PIN LOCATIONS

SECTION V I I

WIRE LIST

7.1 GENERAL

This section contains a wire list which indicates wiring interconnections within the 4001 PCM System. The "Row" and "Col" entries in the wire list refer to row and column contact positions, respectively, in the card reader. Circuit board connections are listed as numeric alpha-numeric reference designations, indicating the circuit board and associated connector pin at which the connector is made. The first digit(s) of the reference designation refers to the card file slot in which the circuit board is located (see Table 5-2), and the remaining (alpha-numeric) portion of the reference designation indicates the connector pin of the circuit board. For example, the reference designation 18ER1 refers to connector pin ER1 of circuit board 070047 (card file slot 18). The location of circuit board connector pins is shown in Figure 7-1.

Wire List.

From	To
21ER1	10AR5
	J4-25
21DR5	10BR4
	J4-26
21CR4	10CR1
	J4-27
21CR3	10DR2
	J4-28
21ER5	10CL5
	J4-29
21ER4	10CR4
	J4-30
21BR3	10EL1
	J4-31
21BR2	10DL4
	J4-32
21FR2	10GR2
	J4-33
21FR1	10GL3
	J4-34
21ER5	10FR4
	J4-35
21ER4	10EL5
	J4-36
21DR4	10FL3
	J4-37
14ER1	10BL3

From	To
14DL5	10BR3
14DR3	10BL4
14CR4	10CL1
14CL1	10BR5
14BR5	10BL5
14BL5	10ER5
14BL2	13FR3
	10EL4
13ER1	10ER2
13DL5	10ER1
13DR3	10DL5
13CR4	10DR3
13BL2	12FR3
12BL2	11FR3
11BL2	10GR1
10BL2	15CR1
10AR4	15BR5
10AR3	15BR4
10AL2	15BR3
10FL5	11AL4
	12AL4
	13AL4
	14AL4

From	To
10GL1	11AL5
	12AL5
	13AL5
	14AL5
10GL2	11BR2
	12BR2
	13BR2
	14BR2
14DL4	15ER4
14EL5	15ER3
14ER5	15ER2
14EL4	15ER1
14CL4	15DR5
14AR5	15DR4
14DR2	15DR3
14CL5	15DR2
13DL4	15DR1
13EL5	15CR5
13ER5	15CR4
13EL4	15CR3
13CL4	15CR2
13AR5	15EL5
13DR2	15EL4
13CL5	15EL3

Wire List (Continued)

From	To
12DL4	15EL2
12EL5	15EL1
12ER5	15DL5
12EL4	15DL4
12CL4	15FL1
12AR5	15FL2
12DR2	15FL3
12CL5	15FL4
11DL4	15FL5
11EL5	15GL1
11ER5	15GL2
11EL4	15GL3
11CL4	15ER5
11AR5	15FR1
11DR2	15FR2
11CL5	15FR3
10GR3	15FR4
9GR1	10BR1
	16EL3
	17EL4
10AL3	15CL5
	20GL2
10DL1	11AL3
	12AL3
	13AL3
	14AL3
	15CL3
	20GL1
8AR2	10AL4
	16FL3
	17AL4
	18FL5
	J4-42
9DL5	16BL2
8AR4	16BL3
	17DL1
	20DR3
8PR2	18FR3
8BR5	18GL1
8CL2	18CL4
8CR2	18AL3
8AR5	16BR2
8BL3	20EL4
8BL2	19FR3
8CR4	19GL1
8CL5	19CL4
8DR2	19AL3
8CR3	16AL5
8AL3	9BR2
8AL5	9AL5
S13F-1	9BR5
	18CR2
	J4-1
S13F-$\bar{1}$	9CL4
	17AR2
	18BL5
S13F-2	9BR1
	18CL2
	J4-2
S13F-$\bar{2}$	9CR4
	17AR4
	18CL1
9BL2	10FR3
9CR3	16BR1
9FR3	10FL4
	16DR5
	17ER5
	20GR1
9FR2	16BR3
9FL1	16AL4
	17BL2
	J4-44
9DR3	10FR5
9FL3	16FR3
9EL1	10BR2

Wire List (Continued)

From	To
S13F-4	9PL5
	18CL3
	J4-3
S13F-$\bar{4}$	9CL5
	17AR3
	18CL5
S13F-8	9DR2
	18CR3
	J4-4
S13F-$\bar{8}$	9DL1
	17BR1
	18BR2
17PL5	18CR4
17BR5	18DR2
17CL1	18GR2
17CR4	18GR3
S13D-$\bar{1}$	17CL5
	18EL4
S13D-$\bar{2}$	17DR2
	18ER5
S13D-$\bar{4}$	17AR5
	18EL5
S13D-$\bar{8}$	17CL4
	18DR3
9EL4	20DR5
9EL5	20ER2
9GL3	20ER3
9GR2	20ER4
10AL5	16AL3
Row12,Col 4	17FR1
	20GR2
Row12,Col 3	10BL1
	16DR1
	17BL1
10AR2	16CR5
	17FR3
	20ER5
	J4-46
Row 8,Col 1	11FL2
	20DR4
Row 8,Col 3	11FR4
	20EL3
Row 8,Col 5	11EL3
	20FL1
Row 8,Col 7	11CR5
	20FL2
15CL4	16AR4
15DL1	16AR3
8BL5	16AR2
	17BR2
	19FL5
	J4-43
16BL4	17AL5
16GR2	17GL3
	J4-38
	J105
16GL1	17GL1
	20GL3
16BL5	17ER1
	DS7-1
16BR4	17DL5
	DS8-1
17FL1	20FL3
17DR3	20FR3
	20PL3
17AL3	20PL2
17FL5	20CR5
Row11,Col 10	8BR4
	18DR1
Row11,Col 11	8BL4
	19DR1
S13C-$\bar{1}$	19BL5
	20BR3
S13C-$\bar{2}$	19CL1
	20AR2
S13C-$\bar{4}$	19CL5
	20AR4
S13C-$\bar{8}$	19BR2
	20AR3

Wire List (Continued)

From	To
S13B-$\bar{1}$	19CR4
	20AL2
S13B-$\bar{2}$	19DR2
	20BR1
S13B-$\bar{4}$	19GR2
	20BR4
S13B-$\bar{8}$	19GR3
	20BL4
Row 8,Col 2	11FR2
	20EL2
Row 8,Col 4	11ER2
	20FR1
Row 8,Col 6	11ER4
	20FR2
Row 8,Col 8	11DR1
	20FR4
+5V	18AL5
	19AL5
14FR3	20AR5
16GR1	9GR3
15FR5	15GR1
	15GR2
	15GL4
-24V	15DL2
	21DL2
+24V	15DL3
	21DL3
17FL2	10FL3

From	To
DS1-1	16DR3
DS2-1	16DR4
DS3-1	16ER2
DS4-1	16EL2
DS501	16BR5
DS6-1	17EL5
DS7-1	16BL5
DS8-1	16BR4
DS9-1	21ER2
DS10-1	21DL5
DS11-1	21CL5
DS12-1	21CR2
DS13-1	21CR1
DS14-1	21CL4
DS15-1	21CL3
DS16-1	21BR1
DS17-1	21FR3
DS18-1	21EL2
DS19-1	21-EL1
DS20-1	21ER3
J105	16GR2

From	To
J106	17GR1
	J4-39
M2-+	21AR4
S7-2	21DR1
S6-1	56-3
	16GL3
S5A-$\bar{8}$	15AR5
S5A-$\bar{4}$	15AR4
S5A-$\bar{2}$	15AR2
S5A-$\bar{1}$	15AL2
S5B-$\bar{8}$	16EL5
S5B-$\bar{4}$	16ER5
S5B-$\bar{2}$	16EL4
S5B-$\bar{1}$	16ER4
S5C-$\bar{8}$	16FL2
S5C-$\bar{4}$	16FR2
S5C-$\bar{2}$	16FL1
S5C-$\bar{1}$	16FR1
S5D-$\bar{8}$	15CL1
S5D-$\bar{4}$	15BL4
S5D-$\bar{2}$	15BL2
S5D-$\bar{1}$	15AL5

From	To
S13A-8	19GL3 J4-24
S13A-4	19GR1 J4-23
S13A-2	19DL4 J4-22
S13A-1	19ER1 J4-21
S13A-$\bar{8}$	19DR3
S13A-$\bar{4}$	19EL5
S13A-$\bar{2}$	19ER5
S13A-$\bar{1}$	19EL4
S13B-8	19DL5 J4-20
S13B-4	19FR5 J4-19
S13B-2	19DL1 J4-18
S13B-1	19BR5 J4-17
S13B-$\bar{8}$	19GR3
S13B-$\bar{4}$	19GR2
S13B-$\bar{2}$	19DR2
S13B-$\bar{1}$	19CR4
S13C-8	19CR3 J4-16
S13C-4	19CL3 J4-15
S13C-2	19CL2 J4-14
S13C-1	19CR2 J4-13
S13C-$\bar{8}$	19BR2
S13C-$\bar{4}$	19CL5
S13C-$\bar{2}$	19CL1
S13C-$\bar{1}$	19BL5
S13D-8	18GL3 J4-12
S13D-4	18GR1
S13D-2	18DL4 J4-10
S13D-1	18ER1 J4-9
S13D-$\bar{8}$	18DR3
S13D-$\bar{4}$	18EL5
S13D-$\bar{2}$	18ER5
S13D-$\bar{1}$	18EL4
S13E-8	18DL5 J4-8
S13E-4	18FR5 J4-7
S13E-2	18DL1 J4-6
S13E-1	18BR5 J4-5
S13E-$\bar{8}$	18GR3
S13E-$\bar{4}$	18GR2
S13E-$\bar{2}$	18DR2
S13E-$\bar{1}$	18CR4
S13F-8	18CR3
S13F-4	18CL3
S13F-2	18CL2
S13F-1	18CR2
S13F-$\bar{8}$	18BR2
S13F-$\bar{4}$	18CL5
S13F-$\bar{2}$	18CL1
S13F-$\bar{1}$	18BL5
S7-2	S8-2 S9-2 S10-2 S11-2 S12-2
GND	S5A-C S5B-$\bar{C}$ S5C-$\bar{C}$ S5D-C S6-2 M2-J108

Wire List (Continued)

From	To	From	To	From	To
S13A-C	S13A-$\bar{C}$	GND	DS1-3	J4-8	18DL5
	S7-1		DS2-3		
			DS3-3	J4-9	18ER1
S13B-C	S13B-$\bar{C}$		DS4-3		
	S8-1		DS5-3	J4-10	18DL4
			DS6-3		
S13C-C	S13C-$\bar{C}$		DS7-3	J4-11	18GR1
	S9-1		DS8-3		
			DS9-3	J4-12	18GL3
S13D-C	S13D-$\bar{C}$		DS10-3		
	S10-1		DS11-3	J4-13	19CR2
			DS12-3		
S13E-C	S13E-$\bar{C}$		DS13-3	J4-14	19CL2
	S11-1		DS14-3		
			DS15-3	J4-15	19CL3
S13F-C	S13F-$\bar{C}$		DS16-3		
	S12-1		DS17-3	J4-16	19CR3
			DS18-3		
+5V	DS1-2		DS19-3	J4-17	19BR5
	DS2-2		DS20-3		
	DS3-2			J4-18	19DL1
	DS4-2	+5V	S6-4		
	DS5-2			J4-19	19FR5
	DS6-2	M2-+	J107		
	DS7-2			J4-20	19DL5
	DS8-2	J4-1	18CR2		
	DS9-2			J4-21	19ER1
	DS10-2	J4-2	18CL2		
	DS11-2			J4-22	19DL4
	DS12-2	J4-3	18CL3		
	DS13-2			J4-23	19GR1
	DS14-2	J4-4	18CR3		
	DS15-2			J4-24	19GL3
	DS16-2	J4-5	18BR5		
	DS17-2			J4-25	10AR5
	DS18-2	J4-6	18DL1		
	DS19-2			J4-26	10BR4
	DS20-2	J4-7	18FR5		

Wire List (Continued)

From	To	From	To	From	To
J4-27	10CR1	J4-47	17FR2	P201-5	S4-1
J4-28	10DR2	+24V	SBS-2K	P201-6	S4-6
J4-29	10CL5	GND	SBS-2L	P201-7	S4-5
J4-30	10CR4	-24V	SBS-2N	P201-8	S3-3
J4-31	10EL1	SBS-2P	8CL1	P201-9	R1-2
J4-32	10DL4	+5V	SBS-2R	P201-10	S2-2
J4-33	10GR2	SBS-2S	8BR1	P201-11	S2-5
J4-34	10GL3	SBS-2D	J5-C	P201-12	S2-1
J4-35	10FR4	SBS-2L	J5-S		S2-6
J4-36	10EL5	J7-C	14FR3	P201-13	S2-3 S2-4
J4-37	10FL3	GND	J7-S	P201-14	S4-3
J4-38	16GR2	J8-C	10AL3	P201-15	R1-1
J4-39	17GR1	GND	J8-S	P201-16	R1-3
J4-40		J9-C	21AL2	P201-17	J101
J4-41	8BR2	J9-S	21AL3	P201-18	J108
J4-42	18FL5	P201-1	M1- -	P201-19	J104
J4-43	19FL5	P201-2	M1- +	P201-20	J103
J4-44	16AL3	P201-3	S3-1	P201-21	J102
J4-45	16GL2	P201-4	S3-2 S4-2		
J4-46	17FR3				

Wire List (Continued)

From	To	From	To	From	To
Row 12		Row 11		Row 0	
1	16CL3	---	---	1	18FR4
2	16CR3	2	9CR5	2	18BR3
3	10BL1	3	9BR4	3	18BL4
4	17FR1	4	9BL3	4	18BR4
5	9AL2	5	9CR1	5	18CR1
6	9AR2	6	9BR3	6	18FR2
7	9CL2	7	9AR3	7	18DR5
8	9DR1	8	9BL4	8	18ER4
9	9CL3	9	9CR2	9	18DR4
10	9AR4	10	8BR4	10	18ER2
11	9DR5	11	8BL4	11	18EL2
12	9DR4	12	18BL3	12	18ER3
13	9ER2	13	18AR2	13	18FL1
14	9EL2	14	18AR4	14	18FL2
15	9ER3	15	18AR3	15	18EL3
16	9EL3	16	18AL2	16	19BL3
17	9ER4	17	18FR1	17	19AR2
18	9FR1	18	18BR1	18	19AR4
				19	19AR3
				20	19AL2
				21	19FR1
				22	19BR1

Wire List (Continued)

From	To	From	To	From	To
Row 1		Row 2		Row 3	
1	19FR4	1	14GR1	1	13DR5
2	19BR3	2	14GR3	2	13DR4
3	19BL4	3	14FL1	3	13CR3
4	19BR4	4	14FR1	4	13CL3
5	19CR1	5	14EL2	5	13CR1
6	19FR2	6	14ER3	6	13BL3
7	19DR5	7	14DR5	7	13BR4
8	19ER4	8	14DR4	8	13BR1
9	19DR4	9	14CR3	9	13AR4
10	19ER2	10	14CL3	10	13AR2
11	19EL2	11	14CR1	11	12GR1
12	19ER3	12	14BL3	12	12GR3
13	19FL1	13	14BR4	13	12FL1
14	19FL2	14	14BR1	14	12FR1
15	19EL3	15	14AR4	15	12EL2
16	8CR1	16	14AR2	16	12ER3
21	9FL2	17	13GR1	17	12DR5
22	9FR4	18	13GR3	18	12DR4
		19	13FL1	19	12CR3
		20	13FR1	20	12CL3
		21	13EL2	21	12CR1
		22	13ER3	22	12BL3

Wire List (Continued)

From	To	From	To	From	To
Row 4		Row 5		Row 6	
1	12BR4	---	---	1	14EL3
2	12BR1	---	---	2	14ER4
3	12AR4	---	---	3	14CR5
4	12AR2	---	---	4	14DR1
5	11GR1	5	17AL2	5	14CR2
6	11GR3	6	17BR4	6	14CL2
7	11FL1	7	17BL4	7	14BR3
8	11FR1	8	17BR3	8	14BL4
9	11EL2	9	17BL3	9	14AL2
10	11ER3	10	17CR1	10	14AR3
11	11DR5	11	17CL2	11	13GL3
12	11DR4	12	17CR2	12	13GR2
13	11CR3	13	17CL3	13	13FL2
14	11CL3	14	17CR3	14	13FR2
15	11CR1	15	17DR1	15	13FR4
16	11BL3	16	17CR5	16	13ER2
17	11BR4	17	14GL3	17	13EL3
18	11BR1	18	14GR2	18	13ER4
19	11AR4	19	14FL2	19	13CR5
20	11AR2	20	14FR2	20	13DR1
21	10FL1	21	14FR4	21	13CR2
22	10FR1	22	14ER2	22	13CL2

Wire List (Continued)

From	To	From	To	From	To
Row 7		Row 8		Row 9	
1	13BR3	1	11FL2	1	15AL4
2	13BL4	2	11FR2	2	15BL1
3	13AL2	3	11FR4	3	15BL3
4	13AR3	4	11DR2	4	15BL5
5	12GL3	5	11EL3	5	15AL3
6	12GR2	6	11ER4	6	15AR3
7	12FL2	7	11CR5	7	15BR1
8	12FR2	8	11DR1	8	15BR2
9	12FR4	9	11CR2	9	17DR4
10	12ER2	10	11CL2	10	17DR5
11	12EL3	11	11BR3	11	17ER4
12	12ER4	12	11BL4	12	17EL3
13	12CR5	13	11AL2	13	17ER3
14	12DR1	14	11AR3	14	17EL2
15	12CR2	15	10FL2	15	17ER2
16	12CL2	16	10FR2	16	17FR4
17	12BR3	17	10CR5	17	10EL2
18	12BL4	18	10DR1	18	10ER3
19	12AL2	19	10CR3	19	10EL3
20	12AR3	20	10CL3	20	10ER4
21	11GL3	21	10CR2	21	10DR5
22	11GR2	22	10CL2	22	10DR4

Wire List (Continued)

From	To	From	To	From	To
J3-1	18BL5	J3-23	19EL5		
J3-2	18CL1	J3-24	19DR3		
J3-3	18CL5	J3-25	J4-25		
J3-4	18BR2	J3-26	J4-26		
J3-5	18CR4	J3-27	J4-27		
J3-6	18DR2	J3-28	J4-28		
J3-7	18GR2	J3-29	J4-29		
J3-8	18GR3	J3-30	J4-30		
J3-9	18EL4	J3-31	J4-31		
J3-10	18ER5	J3-32	J4-32		
J3-11	18EL5	J3-33	J4-33		
J3-12	18DR3	J3-34	J4-34		
J3-13	19BL5	J3-35	J4-35		
J3-14	19CL1	J3-36	J4-36		
J3-15	19CL5	J3-37	J4-37		
J3-16	19BR2	J3-38	J4-38		
J3-17	19CR4	J3-39	J4-39		
J3-18	19DR2				
J3-19	19GR2				
J3-20	19GR3				
J3-21	19EL4				
J3-22	19ER5				

SECTION VIII

DRAWINGS

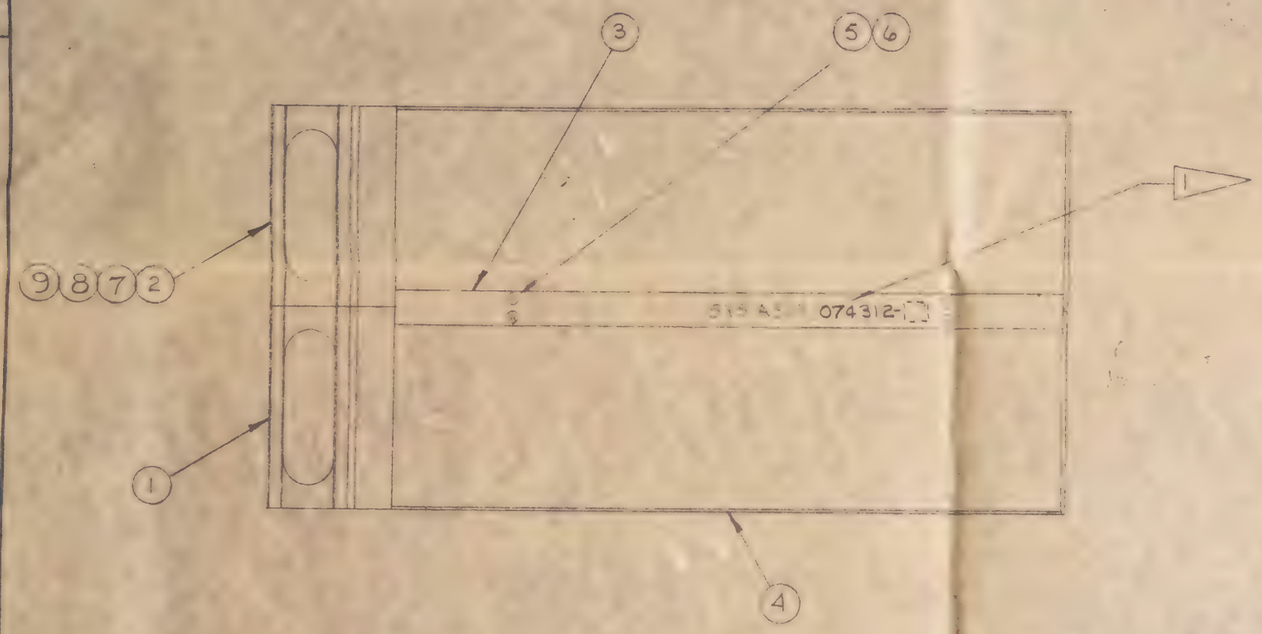
074267	Final Assembly, 4001 PCM System
074245	Unit Assembly, 4001 Card Reader
074246	Front Panel Assembly, 4001 Card Reader
074032	Rear Panel Assembly, 1J-1P
074082	Unit Assembly, 4001 PCM System
074078	Rear Panel Assembly, 2A-20B
074080	Front Panel Assembly, 4001 PCM System
070060	Board Assembly, Data Input and Control Logic
075060	Data Input and Control Logic Diagram
070057	Board Assembly, Data Storage and Control Logic
075057	Data Storage and Control Logic Diagram
070053	Board Assembly 8 Bit Shift Register and Pattern Recognizer
075053	8 Bit Shift Register and Pattern Recognizer Logic Diagram
070003	Board Assembly, Bit Counter and Code Converter
075003	Bit Counter & Code Converter Logic Diagram
070058	Board Assembly, Correlator #1
075058	Correlator #1 Logic Diagram
070052	Board Assembly, SFID Synchronizer
075052	SFID Synchronizer Logic Diagram
070059	Board Assembly, Correlator #2
075059	Correlator #2 Logic Diagram
070047	Board Assembly, Format Counter
075047	Format Counter Logic Diagram
071022	Board Assembly, Error Detector
071035	Error Detector, Schematic Diagram
071016	Board Assembly, D/A-H Converter
071031	D/A-H Converter, Schematic Diagram

SBS-2 Bit Synchronizer

756282	Final Assembly, SBS-2 Bit Synchronizer
756184	Front Panel, SBS-2 Bit Synchronizer
756584	Board Assembly, SBS-2
755381	Board Assembly, Tuning Unit SBS/TU

TA-011157	Meter Board Assembly
TW-012514	Meter Board Control Unit, Schematic Diagram
BA-011460	+8 VDC, +12 VDC Power Supply Board Assembly
BW-012745	+8 VDC, +12 VDC Power Supply Schematic Diagram
BA-011471	-4 VDC, -8 VDC, -12 VDC Power Supply, Board Assembly
BW-012744	-4 VDC, -8 VDC, -12 VDC Power Supply, Schematic Diagram
TA-011577	Integrator and Bit Selector, Board Assembly
TW-012721	Integrator and Bit Selector, Schematic Diagram
TA-011756	DC Restorer and Limiter, Board Assembly
TW-012723	DC Restorer and Limiter, Schematic Diagram
TA-011540	DC Restorer and Limiter, Plug-In Board Assembly
TW-012723	DC Restorer and Limiter, Plug-In Schematic Diagram
TA-011734	VCO Board Assembly
TW-012496	VCO and DC Amplifier Schematic Diagram
TA-012105	Phase Comparator, Board Assembly
TW-015280	Phase Comparator, Schematic Diagram

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:
1. STAMP SYS. ASSY. Nº. AS SHOWN, IN 1/8 HIGH CHARACTERS, USING BLACK INDELIBLE INK.
2. FOR WIRING SEE DWG. 074313

QTY REQD				PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
-4	-3	-2	-1			LIST OF MATERIALS			
1	—	—	—	074311-4		UNIT ASS'Y PCM SYS 4001-111			9
—	1	—	—	074311-3		UNIT ASS'Y PCM SYS 4001-110			8
—	—	1	—	074311-2		UNIT ASS'Y PCM SYS 4001-100			7
A/R	A/R	A/R	A/R	TYPE C(4-1)		LOCTITE	LOCTITE		6
8	8	8	8			SCREW PHMS 4-40			5
2	2	2	2	079022		COVER			4
2	2	2	2	079013		SIDE RAIL LOCK			3
—	—	—	1	074311-1		UNIT ASS'Y PCM SYS 4001-000			2
1	1	1	1	074265-1		UNIT ASS'Y CARD READER			1

REF	DESCRIPTION	QTY

FINAL NEXT ASSY | USED ON
APPLICATION

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8.
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ±.010 .XX ±.02
FRACTIONS ±1/64 ANGLES ±1°
FLATNESS WITHIN .002
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL
FINISH

CONTRACT NO.

		DATE
DRAWN	Lou Kamuyo	3-10-69
CHECKED	[illegible]	3-12-69
DESIGNER	[illegible]	3-12-69
PROJECT ENG	[illegible]	3-12-69
APPROVED	[illegible]	4-18-69

APPROVED
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

FINAL ASS'Y MODEL 4001-XXX-006

SIZE	CODE IDENT.	
C	08539	074312

SCALE NONE | 30-14508 | SHEET

GRAPHIC CONTROLS CORP., BROOKLYN, N.Y. 11217 REMOVED NO. 44GM 13555

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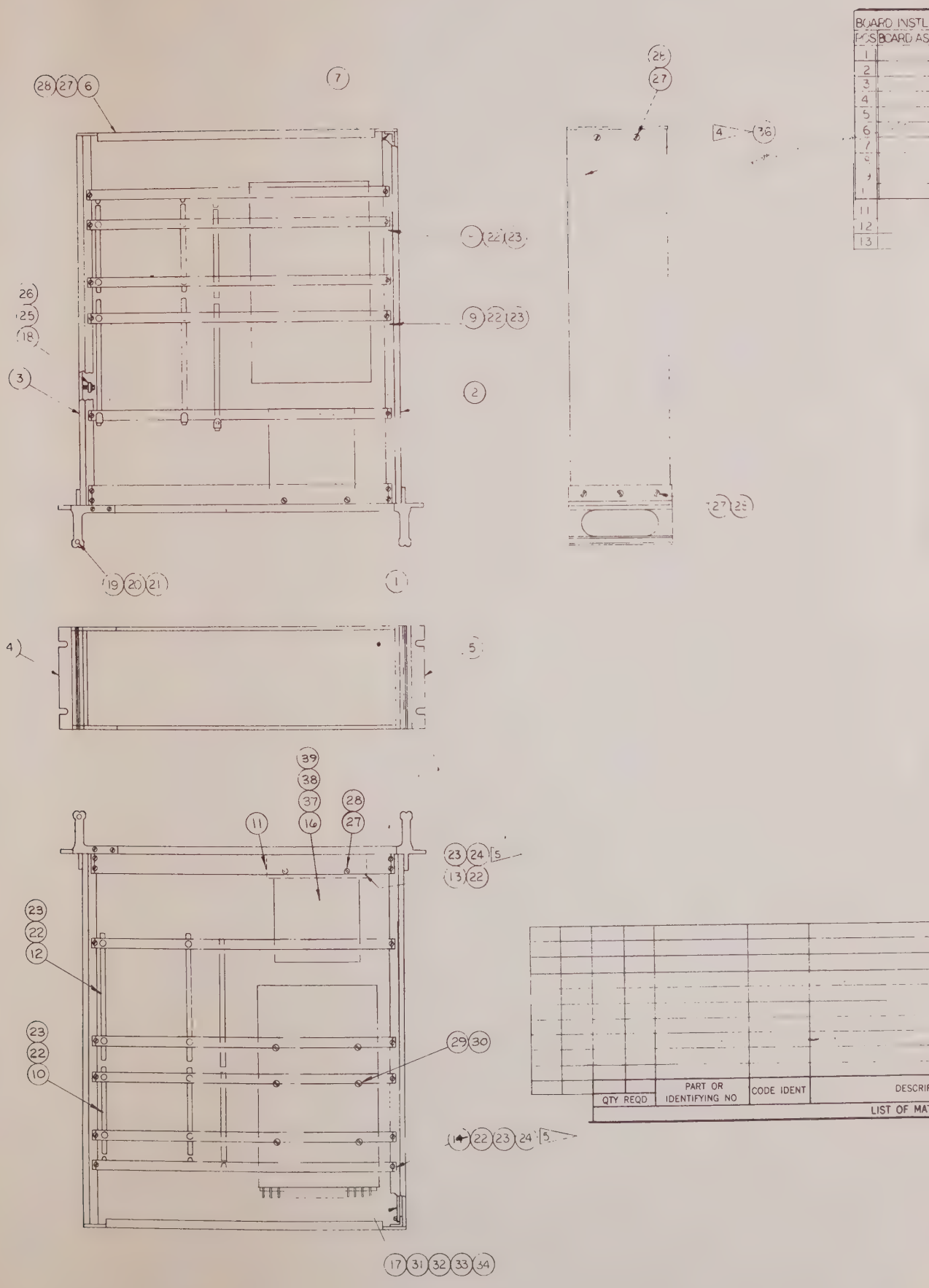
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QTY REQD
PART OR IDENTIFYING NO
CODE IDENT
DESCRIP
LIST OF MA

NOTES:

1. ASSEMBLE PER DCS SPEC QS5000 SERIES.
2. FOR WIRING SEE FINAL ASSY.
3. FOR LOCATION SEE BOARD INSTALLATION CHART.
4. STAMP MODEL AND SERIAL NO. IN 1/8 HIGH CHARACTERS, AFFIX ITEM 36 OVER STAMPING, LOCATE APPROX AS SHOWN.
5. ASSEMBLE SIDE RAILS AND ALL MTG BARS, AFFIX ASSY IN ALIGNING JIGS 074055 THEN DRILL (#40) .062 DIA. HOLES IN SIDE RAILS USING EXISTING HOLES IN ITEMS 13 & 14 AS PILOT HOLES, THEN INSTALL ITEM 24.

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
4			NUT, LOCK #8	CPS		39
4			WASHER, FLAT #8	CPS		38
4			SCREW, F.H. 82° #8-32	CPS		37
1	613361		NAME PLATE			36
A/R	TYPE (4-1)		LACING TAPE			35
2			WASHER, FLAT #4			34
2			SCREW, #4-40 FIL H SLOTTED			33
2	079053		HINGE, REAR PANEL			32
2			NUT, LOCK #4-40			31
6			SCREW, PH #10-32	CPS		30
6			WASHER, LOCK #10	CPS		29
14			WASHER, LOCK #6			28
18			SCREW, #6-32 PHMS			27
3			NUT, LOCK #6-32			26
9			WASHER, FLAT #6			25
16	MS16562-92		PIN 1/16 X 3/8			24
28			WASHER, LOCK #4			23
28			SCREW, #4-40 PHMS			22
2	AS826034-3140		WASHER, FLAT NYLON			21
2			SETSCREW #6-32 X 1/8 LG			20
2	079020		HINGE PIN			19
4	079053		CABLE CLAMP			18
2	431		SHOULDER SCREW	PIC		17
1	074139-1		CARD READER			16
1	074141		POWER SUPPLY			15
2	079103		MTG BAR GUIDE			14
2	079101		MTG BAR			13
1	079106		MTG GUIDE ASSY			12
1	079102-1		CARD READER BRACKET			11
1	079107		MTG GUIDE ASSY			10
1	079104		MTG GUIDE ASSY			9
1	079105		MTG GUIDE ASSY			8
2	079036		MTG BRACKET, REAR			7
1	074032-1		REAR PANEL ASSY 1U-1P			6
1	079043-01		HANDLE			5
1	079044-01		HANDLE, HINGED			4
1	079032		SIDE RAIL, LEFT			3
1	079021		SIDE RAIL, RIGHT			2
1	074240-1		FRONT PANEL ASSY			1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ± .005 .XX ± .01
FRACTIONS ± 1/64 ANGLES ± 1°
FLATNESS WITHIN 0.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL —

FINISH —

074268	MOD. 4001A
074267	MOD. 4001
NEXT ASSY	USED ON

APPLICATION

CONTRACT NO.

		DATE
DRAWN	[illegible]	1-21-69
CHECKED	[illegible]	1-22-69
DESIGNER	[illegible]	1-22-69
PROJECT ENG	[illegible]	1-22-69
APPROVED	[illegible]	1-22-69

APPROVED

APPROVED

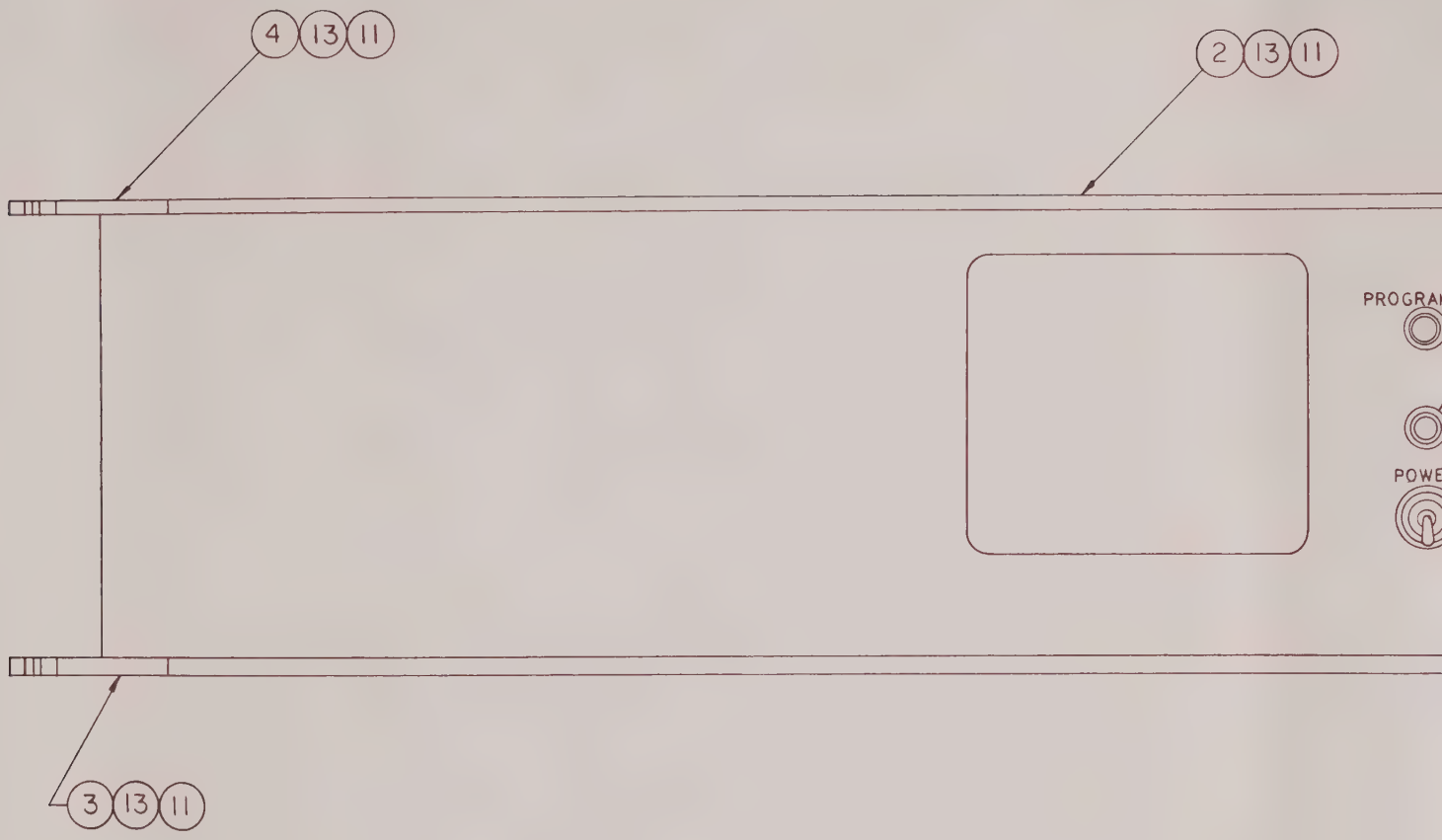
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

UNIT ASSY
CARD READER
MODEL 4001 & 1001A

SIZE	CODE IDENT	
D	08539	074265

SCALE NONE E259 SHEET —

074265


4 13 11
2 13 11
PROGRA
POWE
3 13 11

ITEM	SYMBOL	SPECIFICATION OR VENDOR	DESCRIPTION	CODE IDENT.	PART OR IDENTIFYING NO.	QTY REQD
						-1
13		STEEL	SCREW PH. #4-40, BLK. OXIDE			10
12			WASHER, FLAT #4			6
11			WASHER, LOCK EXT. TOOTH #4			12
10		CPS	SCREW PH, #4-40			2
9	S1		SWITCH, TOGGLE, BLK. BAT.		83050	1
8			PANEL LIFT		079081	1
7		ARROWHART	NUT, KNURLED, BLK.		8991-3	1
6	D61 & D52	TEC	INDICATOR GRN		MSTL-D005-BL-5	2
5		SOUTHCO	FASTENER		62-99-209-10	1
4			HINGE TOP		079018	1
3			HINGE BOTTOM		079019	1
2			TRIM BAR		079037	2
1			FRONT PANEL		074247-1	1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.

		DATE
DRAWN	D.R. WEST	11-22-68
CHECKED	J.K. BURLINSON	11-22-68
DESIGNER	J.K. BURLINSON	11-22-68
PROJECT ENG	R. Gormley	11-25-68
APPROVED		

MATERIAL ±
APPROVED

FINISH ±
APPROVED

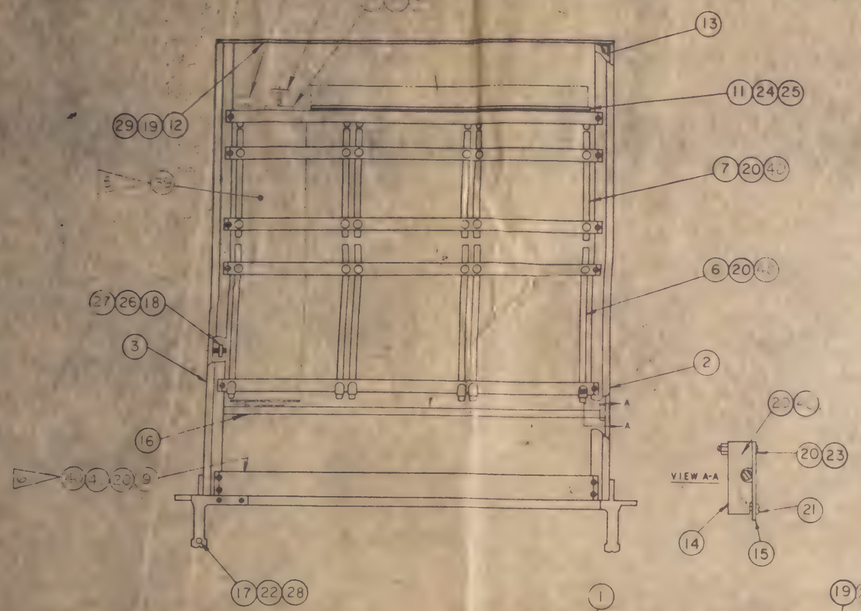
074245
NEXT ASSY | USED ON
APPLICATION

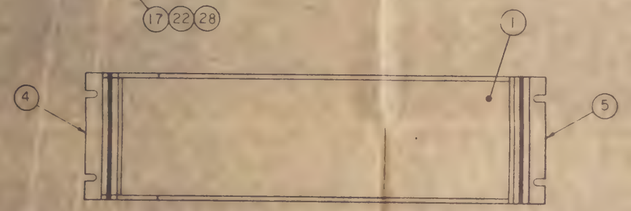
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

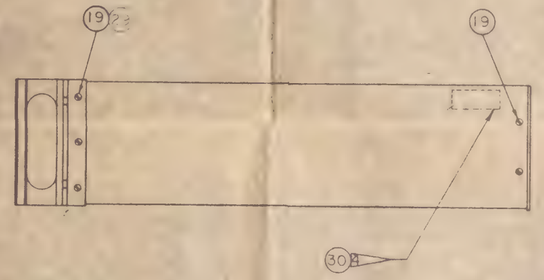
FRONT PANEL ASSY
CARD READER
MODEL 4001

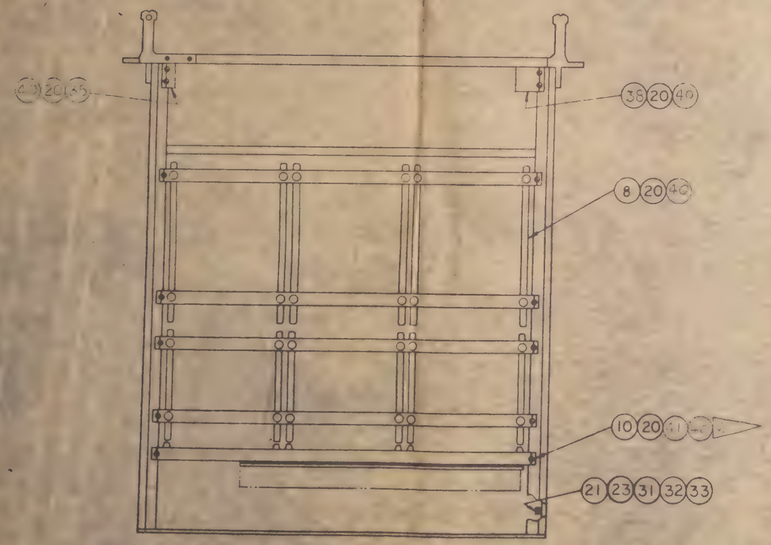
SIZE D | CODE IDENT. 08539 | 074246

SCALE: FULL | 50 14083 | SHEET C-12









BOARD INSTALLATION CHART					
POS	BOARD ASSY No.	-1 000	-2 100	-3 110	-4 111
1					
2					
3					
4	756282 (SBS-2)				
5					
6					
7					
8	070060				
9	070003				
10	070057				
11	070058				
12					
13					
14	070058				
15	071022				
16	070058				
17	070058	-	-		
18	070047				
19	070047	-			
20	070052	-	-	-	-
21	071016				
22	070188				
23	070183				
24	BLANK				
25					
26					
27					
28					
29					
30	BLANK				

NOTES:
1. ASSEMBLE PER DCS WORKMANSHIP MANUAL AS832011.
2. FOR WIRING SEE DWG. NO. 074313
3. FOR LOCATION SEE BOARD INSTALLATION CHART.
4. STAMP MODEL & SERIAL NO. IN 1/8 HIGH CHARACTERS. AFFIX ITEM 30 OVER STAMPING, LOCATE APPROX. AS SHOWN. MODEL No. EXAMPLE (4001-000)
5. SBS-2 (ITEM 39) TUNING UNIT(S) TO BE SPECIFIED ON P.O. OR W.O.
6. ASSEMBLE SIDE RAILS & ALL MTG. BARS, AFFIX ASS'Y IN ALIGNING JIGS #074055. THEN DRILL (12) .062 DIA. HOLES IN SIDE RAILS USING EXISTING HOLES IN ITEMS 9 & 10 AS PILOT HOLES; THEN INSTALL ITEM 41.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

-4	-3	-2	-1	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
			1		5033		MOUNTING PLATE			60
1	1	1	1		071022		BD. ASS'Y ERROR DETECTOR		5	58
										57
1	1	1	1		071016		D/A-H			56
1	1	1	1		070060		4002 DATA INPUT & CONT. LOGIC			55
1	1	-	-		070059		CORRELATOR #2			54
1	1	1	1		070058		CORRELATOR #1			53
1	1	1	1		070057		DATA STOR & CONT. LOGIC			52
										51
										50
										49
1	4	4	4		070055		8 BIT SHIFT REG & PAT. RECG			48
	-	-	-		070052		SFID SYCHRONIZER			47
										46
										45
2	2	2	2		070188		OUTPUT DRIVER			44
2	2	2	1		070047		FORMAT COUNTER			43
1	1	1	1		070003		BD. ASS'Y BIT CTR & CODE CONVERTER		3	42
12	12	12	12		MS16562-192		PINS, 1/16 x 3/8			41
34	34	34	34				WASHER, LOCK #4			40
5 1	1	1	1		756282		SBS-2 UNIT		3	39
1	1	1	1		079083		PANEL STOP (LIFT)			38
1	1	1	1		079033		CONNECTOR BRACKET			37
			1		143-015-01		CONNECTOR	AMPHENOL		36
			1		079075		PANEL STOP			35
A/R	A/R	A/R	A/R		TYPE C (4-1)		LOC TITE	LOCTITE		34
4	4	4	4				WASHER, FLAT #4			33
2	2	2	2				SCREW, #4-40 FH 100° SLOTTED			32
2	2	2	2		079028		HINGE, REAR PANEL			31
1	1	1	1		013361		NAME PLATE			30
10	10	10	10				WASHER, LOCK #6-32			29
2	2	2	2		AS826034-31-40		WASHER, FLAT NYLON			28
6	6	6	6				NUT, LOCK #6-32			27
12	12	12	12				WASHER, FLAT #6			26
14	14	14	14				SCREW, NYLON #4-40			25
A/R	A/R	A/R	A/R				WASHER, NYLON #4 x 1/4 OD			24
5	5	5	5				NUT, LOCK #4-40			23
2	2	2	2				SETSCREW #6-32 x 1/8 LG			22
3	3	3	3		4310		SHOULDER SCREW	PIC		21
37	37	37	37				SCREW, #4-40 PHMS			20
18	18	18	18				SCREW, #6-32 PHMS			19
6	6	6	6		079053		CABLE CLAMP			18
2	2	2	2		079020		HINGE PIN			17
1	1	1	1		079054		CARD HOLDER BAR			16
1	1	1	1		079055		BAR HOLDER			15
1	1	1	1		079056		BRACKET, CARD HOLDER			14
2	2	2	2		079036		MTG BRACKET REAR			13
1	1	1	1		074072-1		REAR PANEL ASS'Y 2A-20B			12
1	1	1	1		079045-4		CONNECTOR PLATE			11
2	2	2	2		079003		MTG BAR GUIDE			10
1	1	1	1		079026		MTG BAR			9
1	1	1	1		079014		MTG GUIDE ASS'Y			8
2	2	2	2		079011		MTG GUIDE ASS'Y			7
1	1	1	1		079010		MTG GUIDE ASS'Y			6
1	1	1	1		079043-01		HANDLE			5
1	1	1	1		079044-01		HANDLE HINGED			4
1	1	1	1		079032		SIDE RAIL LEFT			3
1	1	1	1		079021		SIDE RAIL RIGHT			2
1	1	1	1		074080-01		FRONT PANEL ASS'Y			1

LIST OF MATERIALS

REF.	DESCRIPTION	QTY

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON
XXX ± .005 XX ± .01
FRACTIONS ± 1/64 ANGLES ± 1°
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX
MATERIAL
FINISH

074312	074312
NEXT ASSY	USED ON
APPLICATION	

CONTRACT NO.

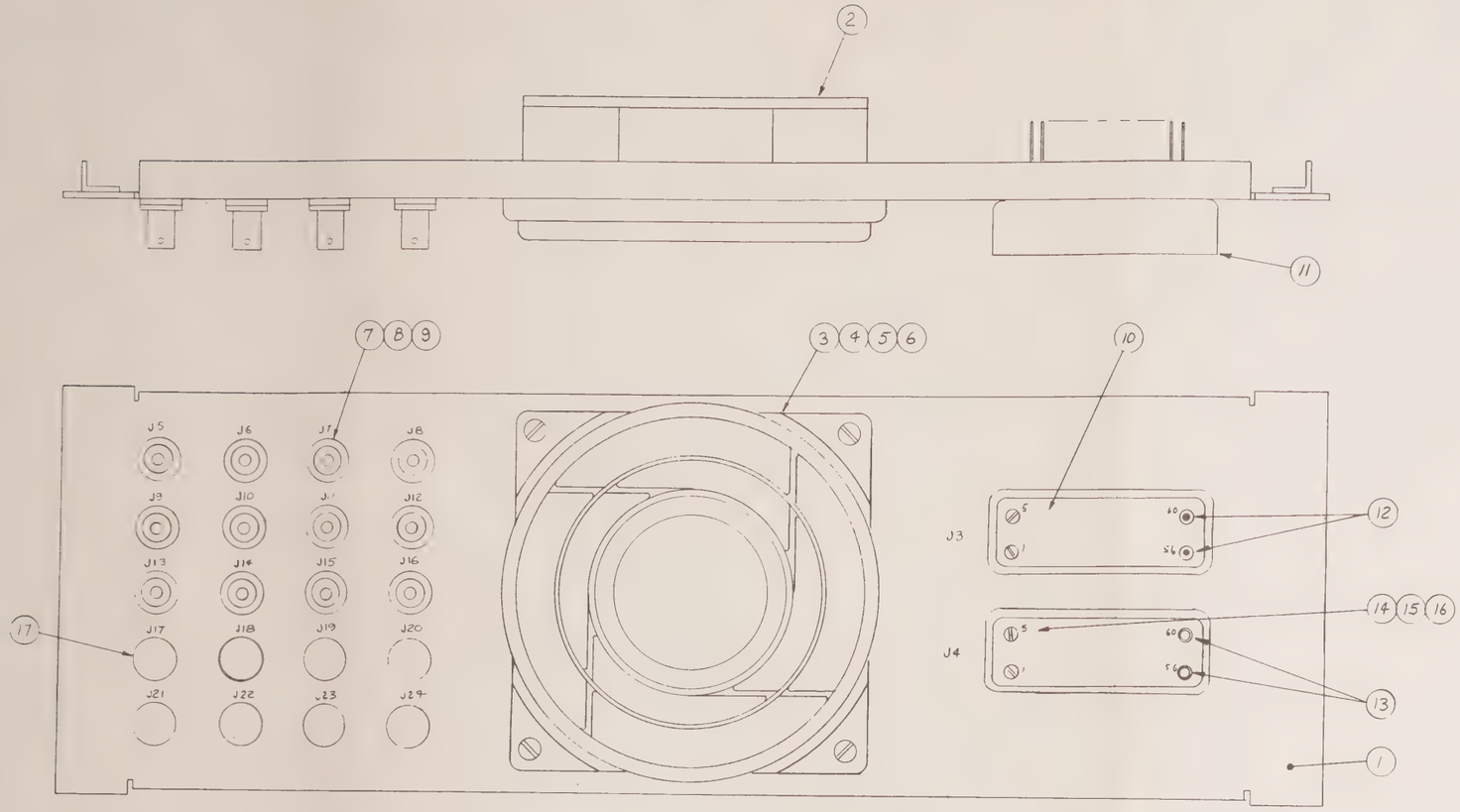
	DATE
DRAWN	3-11-69
CHECKED	3-12-69
DESIGNED	3-12-69
PROJECT ENG	3-12-69
APPROVED	
APPROVED	
APPROVED	

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

UNIT ASS'Y
PCM SYSTEM
MODEL 4001-XXX-006

SIZE	CODE IDENT	
D	08539	074311

SCALE NONE SOJ460B SHEET



074078-1 SHOWN

NOTES:

1. ASSEMBLE PER DCS WORKMANSHIP MANUAL AS832011.
2. REF. MATING CONNECTOR FOR ITEM 10 IS 582459-1 CONTACTS-66272-5, COVER & CABLE CLAMP-200532-2, HOOD-202394-2, JACKSCREWS-582360-3, CORNER GUIDE PIN-200833-4 & SOCKET-200835-4, ALL BY AMP. INC.
3. YELLOW CAD. PER MIL Q.Q.P-416a, TO BE SPECIFIED TO VENDOR.
4. REF. MATING CONN. ITEM 7 IS FXR-13925

12	-	8	D2724 L.C.S.		HOLE PLUG	STIMPSON	3	17
4	4	4			WASHER, FLAT CPS#4			16
4	4	4			NUT, LOCK CPS#4			15
4	4	4			SCREW P.H. CPS#4			14
2	2	2	200835-4		CORNER GUIDE SOCKET	AMP INC.		13
2	2	2	200833-4		CORNER GUIDE PIN	↕ ↕		12
2	2	2	201390-5		HOOD	↕ ↕		11
2	2	2	583048-2		CONNECTOR	AMP. INC.	J3 & J4	10
16	40	24	10221-N		SHOULDER WASHER	MILTON ROSS		9
8	20	12	1497		SOLDER LUG	H. H. SMITH		8
8	20	12	UG657/U		CONNECTOR			7
4	4	4			WASHER, FLAT CPS#6			6
4	4	4			NUT, LOCK CPS#6			5
4	4	4			SCREW P.H. CPS#6			4
1	1	1	20757		GRILLE	ROTRON		3
1	1	1			FAN MUFFIN VENTURI	ROTRON		2
1	1	1	079088		SUB ASS'Y REAR PANEL			1
-3	-2	-1	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
	QTY REQD							

LIST OF MATERIALS

MULTIPLE	
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX — # .XX — #
FRACTIONS — # ANGLES — #
FLATNESS WITHIN ⌒
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX
MATERIAL — #
FINISH — #

CONTRACT NO.

DRAWN		DATE 2-19-68
CHECKED	J K BURLINSON	2-21-68
DESIGNER	J K BURLINSON	2-21-68
PROJECT ENG.		2-21-68
APPROVED		2-4-68
APPROVED		
APPROVED		

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

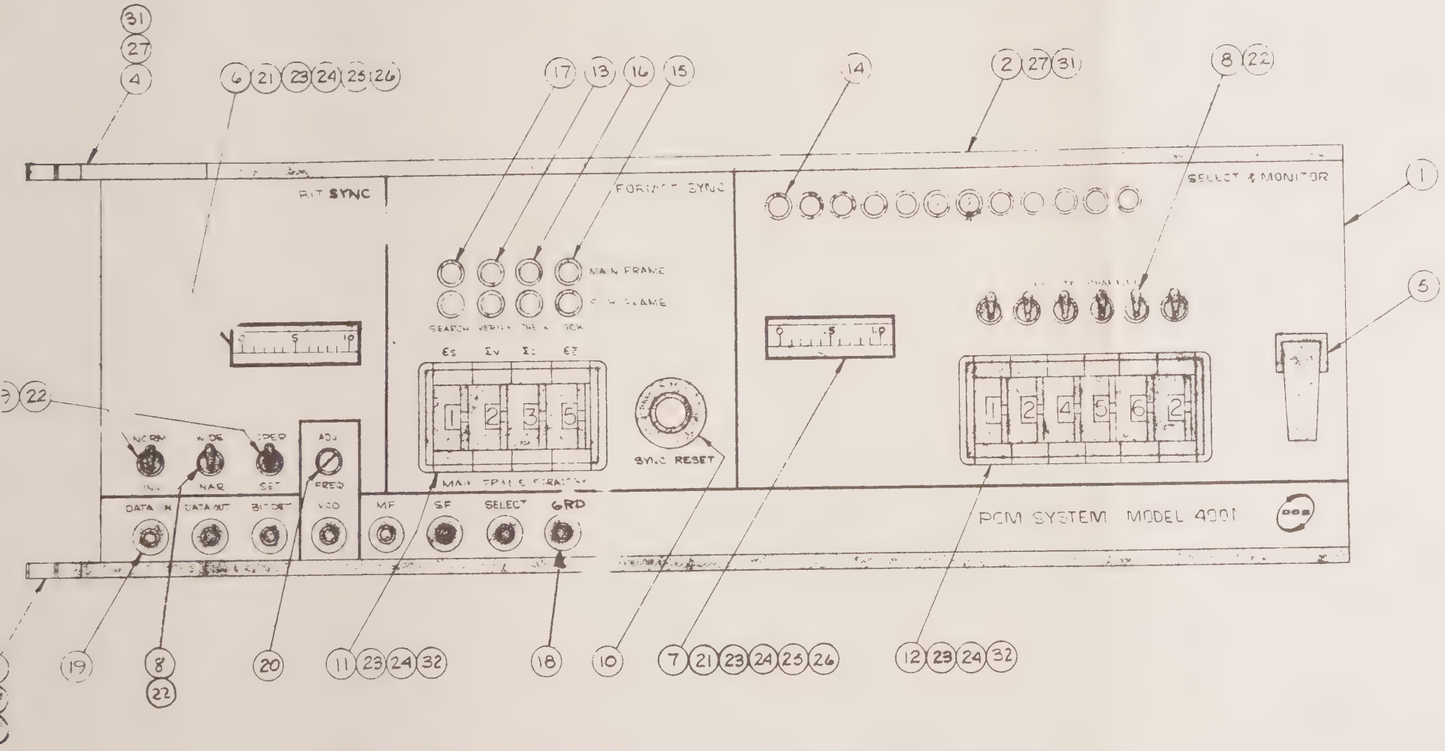
REAR PANEL ASS'Y
2A-20B

SIZE	CODE IDENT.	
D	08539	074078

SCALE: FULL E 259 SHEET

NOTES:

1. SEE WIRE LIST No. 074039 FOR LOCATION.



QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL
48	IN3067		DIODE		
12			WASHER, LOCK EXT. TOOTH #4		
A/R	TYPE C (4-1)		LOCTITE	LOCTITE CORP.	
2			SCREW, PH 4-40	CPS	
1	079081		PANEL LIFT		
10			SCREW, PH 4-40 BLK. OXIDE	STEEL	
4			WASHER, FLAT #2		
4			SCREW, PH 2-56		
14			WASHER, FLAT #4		
12			NUT, LOCK 4-40		
9			DRESS NUT, KNURLED, BLK. 1/4-40		
2	079067-2		BRACKET, METER		
1	C5704-6		POTENTIOMETER 10K ±10%	IRC	R1
7	1509-102		TEST JACK RED	H.H. SMITH	J101-J108
1	1509-103		TEST JACK BLK	H.H. SMITH	J109
2	MSTL-D005-BL-1		INDICATOR RED	TEC	DS1 & DS6
2	-4		YEL		DS3 & DS7
2	-5		GRN		DS4 & DS8
12	-9		WHT		DS9-DS20
2	MSTL-D005-BL-11		INDICATOR ORN.	TEC	DS2 & DS5
1	5638-6		THUMBWHEEL	DIGITRAN	S1B
1	5-D-186		THUMBWHEEL	DIGITRAN	S5
1	MS25089-8C		SWITCH, MOMENTARY	CONTROLS CO.	S6
2	TS6-N8		SWITCH, TOGGLE BLK. BAT	ARROW-HART	S1, S2 & S4
7	TS 3-N8		SWITCH, TOGGLE BLK. BAT	ARROW-HART	S3, S7-S
1	074027		METER		M2
1	010784		METER		M1
1	62-99-209-10		FASTENER	SOUTHCO	
1	079018		HINGE, TOP		
1	079019		HINGE, BOTTOM		
2	079037		TRIM BAR		
1	074044		FRONT PANEL		

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
XXX ±, .XX ±
FRACTIONS ±, ANGLES ±
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX
MATERIAL
FINISH

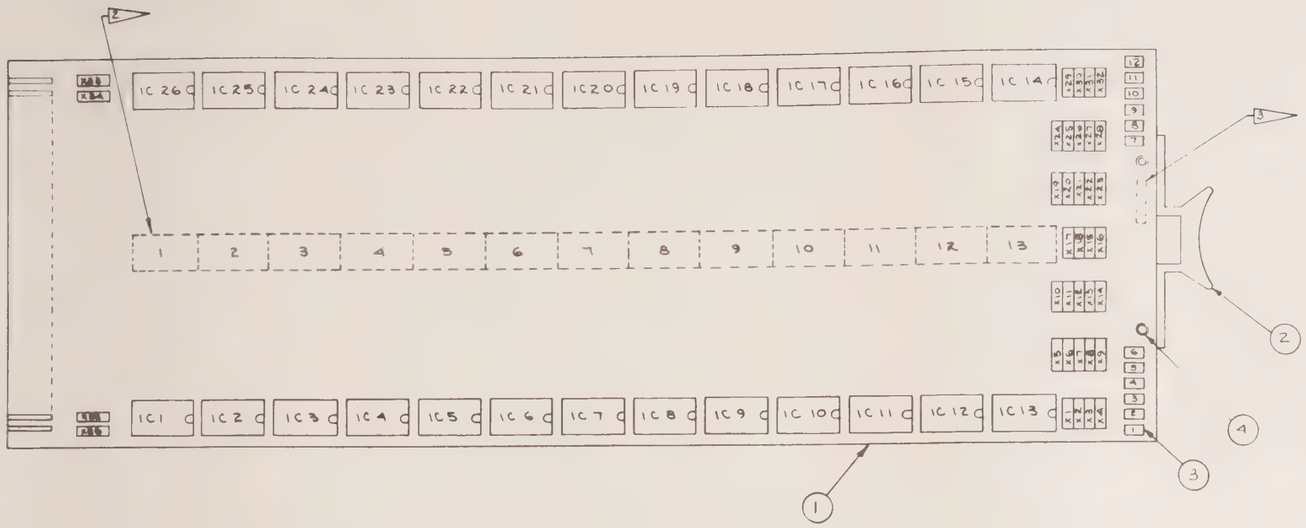
CONTRACT NO.
DRAWN JKB DATE 7-30-68
PROVED

DATA-CONTROL SYSTEMS INC.

FRONT PANEL ASS'Y
PCM SYSTEM
MODEL 40C

NEXT ASSY	USED ON
074082	MOD 400
APPLICATION	

SIZE	CODE IDENT.	
D	08539	074080
SCALE FULL	5.259	SHEET



IC POS. CHART	
IC 1	SN7451N
2	SN7402N
3	SN7440N
4	SN7400N
5	SN15846N
6	SN7451N
7	SN7474N
8	SN7440N
9	SN7400N
10	SN7440N
11	SN7400N
12	——
13	——
14	——
15	——
16	——
17	——
18	——
19	——
20	——
21	——
22	——
23	——
24	——
25	——
IC 26	——

COMP POS. CHART	
X1	1K
X2	——
X3	1K
X4	1K
X5	——
X6	1K
X7	1K
X8	——
X9	1K
X10	1K
X11	——
X12	——
X13	——
X14	——
9 X15	JUMP
X16	——
X17	——
X18	1K
X19	——
X20	——
X21	——
X22	——
X23	——
X24	——
X25	——
X26	——
X27	——
X28	——
X29	——
X30	——
X31	——
X32	——
4 X33	JUMP
X34	.1UF 25V
X35	.1UF 25V
4 X36	JUMP

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE #070060 REV A
2. REPAIR PAD SECTIONS 1-13.
3. STAMP ASSEMBLY NR IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE #22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075060
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM 6 IN "A" HOLES.
9. INSTALL THRU JUMPER IN COMPONENT #15

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
1	SN15846N		IC	T.I.		13
1	SN7474N		IC	T.I.		12
2	SN7451N		IC	T.I.		11
3	SN7440N		IC	T.I.		10
1	SN7402N		IC	T.I.		9
8	SN7400N		IC	T.I.		8
8	MS35350-8		RESISTOR 1/4W, 10%, 1K			7
A/R	016467		CONNECTION PIN			6
2	3C023		CAPACITOR .1UF 25V	SPRAGUE		5
2	1200-5-02		RIVET	CTC		4
12	8046-1		TEST JACK	AUGAT	E1-E12	3
1	SAE 6200		CARD PULL	STAMFORD APPLIED		2
1	070009		BOARD SUB-ASSY			1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
XXX —/— XX —/—
FRACTIONS —/— ANGLES —/—
FLATNESS WITHIN ⌒
HOLE TOLERANCE PER D C S SPECIFICATION AS-8140/8, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.
DRAWN RPW DATE 6-21-68
CHECKED
ENGINEER
PROJECT ENG
APPROVED
MATERIAL —/—
APPROVED
FINISH —/—
APPROVED

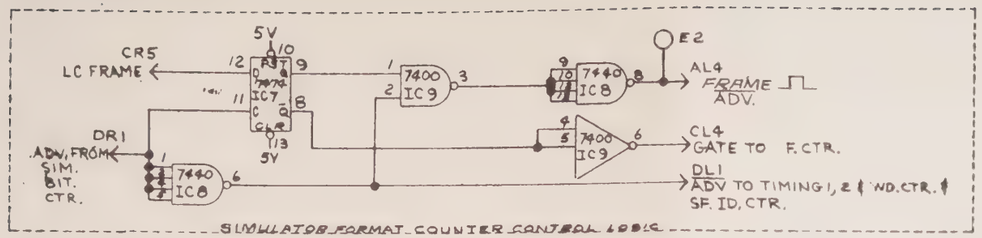
NEXT ASSY | USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

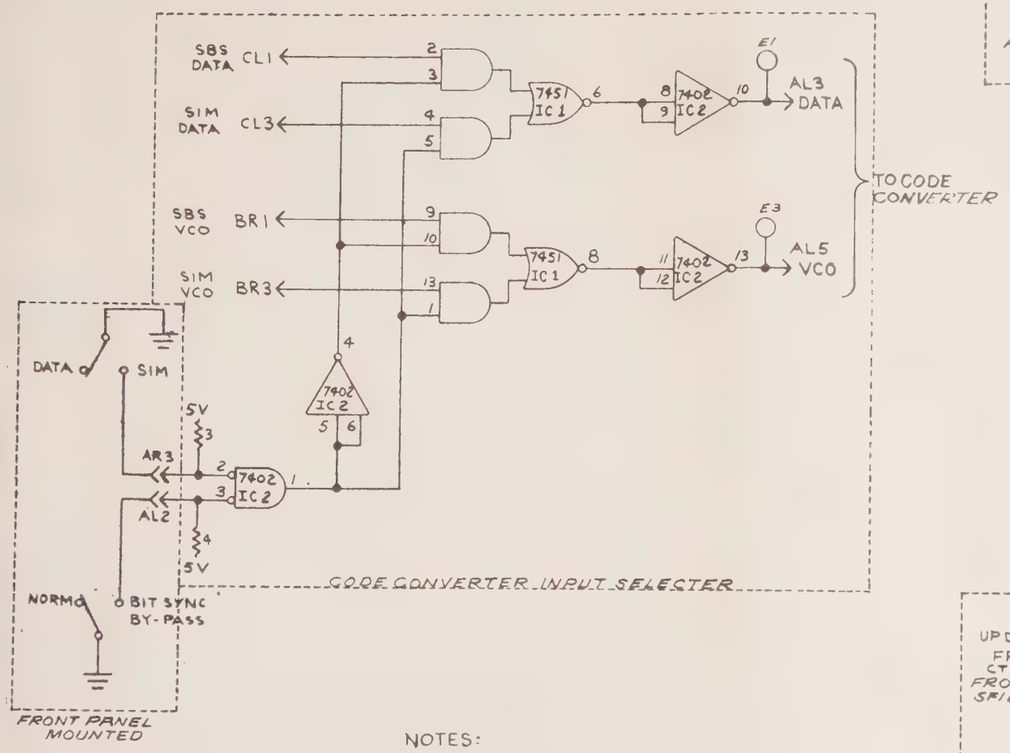
BOARD ASS'Y
DATA INPUT & CONTROL LOGIC

SIZE D | CODE IDENT. 08539 | 070060

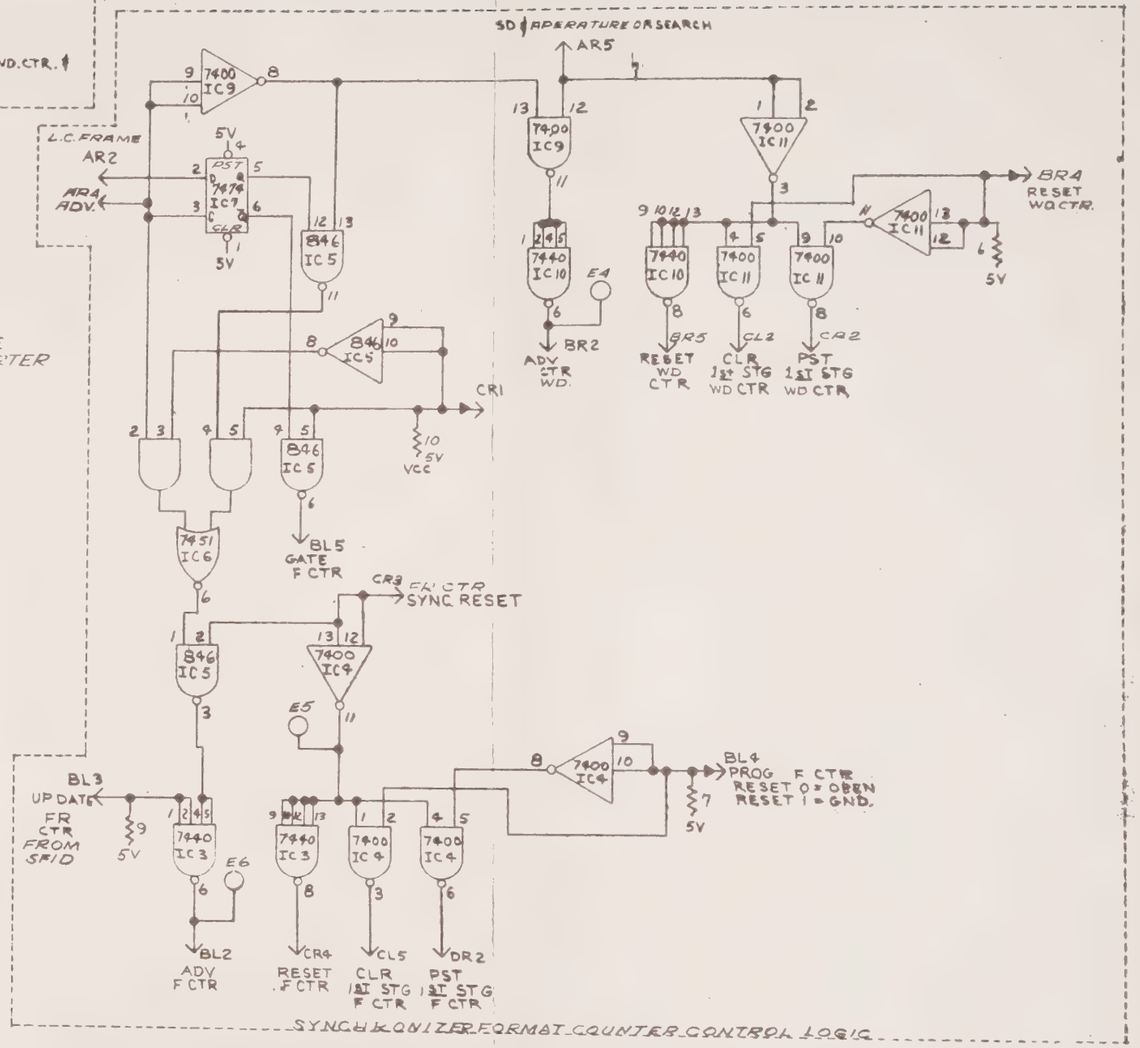
SCALE —/— SHEET —/—



SIMULATOR FORMAT COUNTER CONTROL LOGIC



CODE CONVERTER INPUT SELECTER



SYNCHRONIZER FORMAT COUNTER CONTROL LOGIC

NOTES:

1. → INDICATES PROGRAMMEL LINE
2. 7400, 7402, 7440, 7451, & 7474 ARE PREFIXED BY SN & SUFFIXED BY N EX. (SN 7474 N)

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

070060	
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
.XXX —″— .XX —″—
FRACTIONS —″— ANGLES —″—
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-#14018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL —″—

FINISH —″—

CONTRACT NO.

DRAWN — DATE 5-1-68

CHECKED — DATE 7/12/68

DESIGNER

PROJECT MGR — DATE 7-15-68

APPROVED

APPROVED

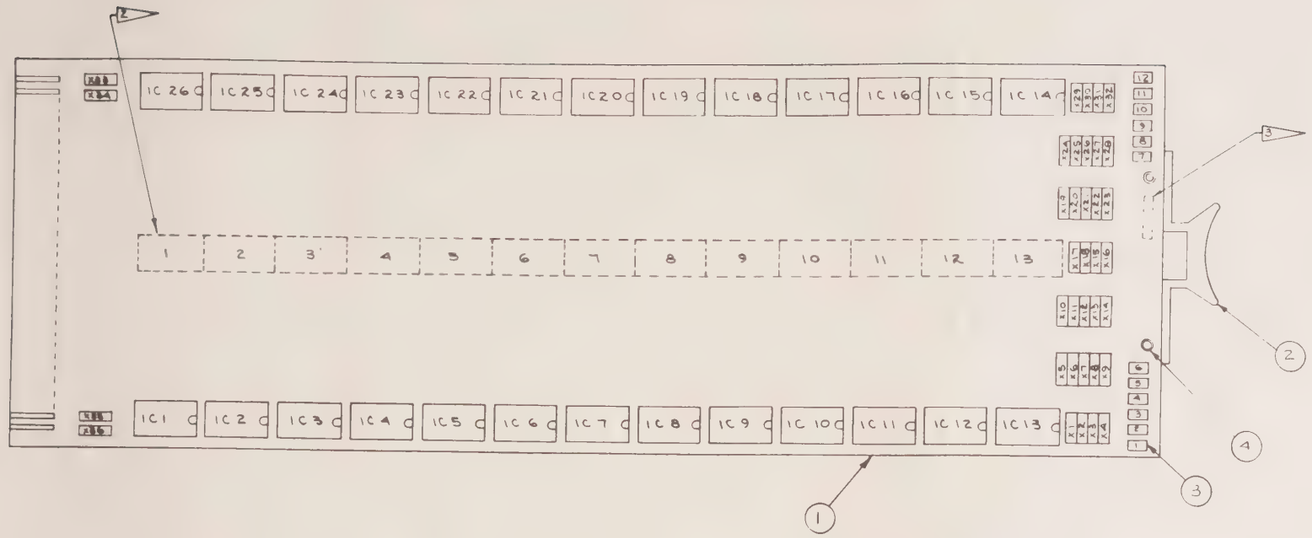
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC DATA INPUT & CONTROL

SIZE	CODE IDENT.	
C	08539	075060

SCALE —″— SHEET —″—



IC POS. CHART	
IC 1	SN7440N
2	SN7400N
3	SN7474N
4	SN7402N
5	SN7400N
6	SN7410N
7	SN7474N
8	SN7440N
9	SN7474N
10	SN7440N
11	SN7474N
12	SN7440N
13	——
14	——
15	SN7400N
16	SN7440N
17	SN7474N
18	SN7440N
19	SN7474N
20	SN7440N
21	SN7474N
22	SN7440N
23	SN15862N
24	SN15862N
25	SN7474N
IC 26	SN7400N

COMP POS. CHART	
X1	——
X2	——
X3	——
X4	——
X5	——
X6	——
X7	——
X8	——
X9	——
X10	——
X11	1K
X12	
X13	
X14	
X15	
X16	
X17	
X18	
X19	
X20	
X21	
X 22	1K
X23	——
X24	——
X25	1K
X26	
X27	
X28	1K
X29	——
X30	——
X31	——
X82	——
X 33	JUMP
X34	.1UF 25V
X35	.1UF 25V
X 36	JUMP

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE #070057 REV A
2. REPAIR PAD SECTIONS 1-13.
3. STAMP ASSEMBLY NO IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE #22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075057
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM 6 IN "A" HOLES.

ITEM	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL
13	16	MS35350-8		RESISTOR 1/4W, 10% 1K		
12	2	SN15862N		IC	T.I.	
11	8	SN7474N		↕	↕	
10	8	SN7440N		↕	↕	
9	1	SN74ICN		↕	↕	
8	1	SN7402N		↕	↕	
7	4	SN7400N		IC	T.I.	
6	A/R	016467		CONNECTION PIN		
5	2	30023		CAPACITOR .1UF 25V	SPRAGUE	
4	2	1200-5-C2		RIVET	CTC	
3	12	8046-1		TEST JACK	AUGAT	E1-E12
2	1	SAE 6200		CARD PULL	STANFORD APPLIED	
1	1	079009		BOARD SUB-ASSY		
	-1					

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON
.XXX —— .XX ——
FRACTIONS —— ANGLES ——
FLATNESS WITHIN ~
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES. REMOVE BURRS .015 MAX
MATERIAL ——
FINISH ——

CONTRACT NO.

		DATE
DRAWN	RG	1-68
CHECKED	RPW	2-68
DESIGNER		
PROJECT ENG	RG	1-68
APPROVED		

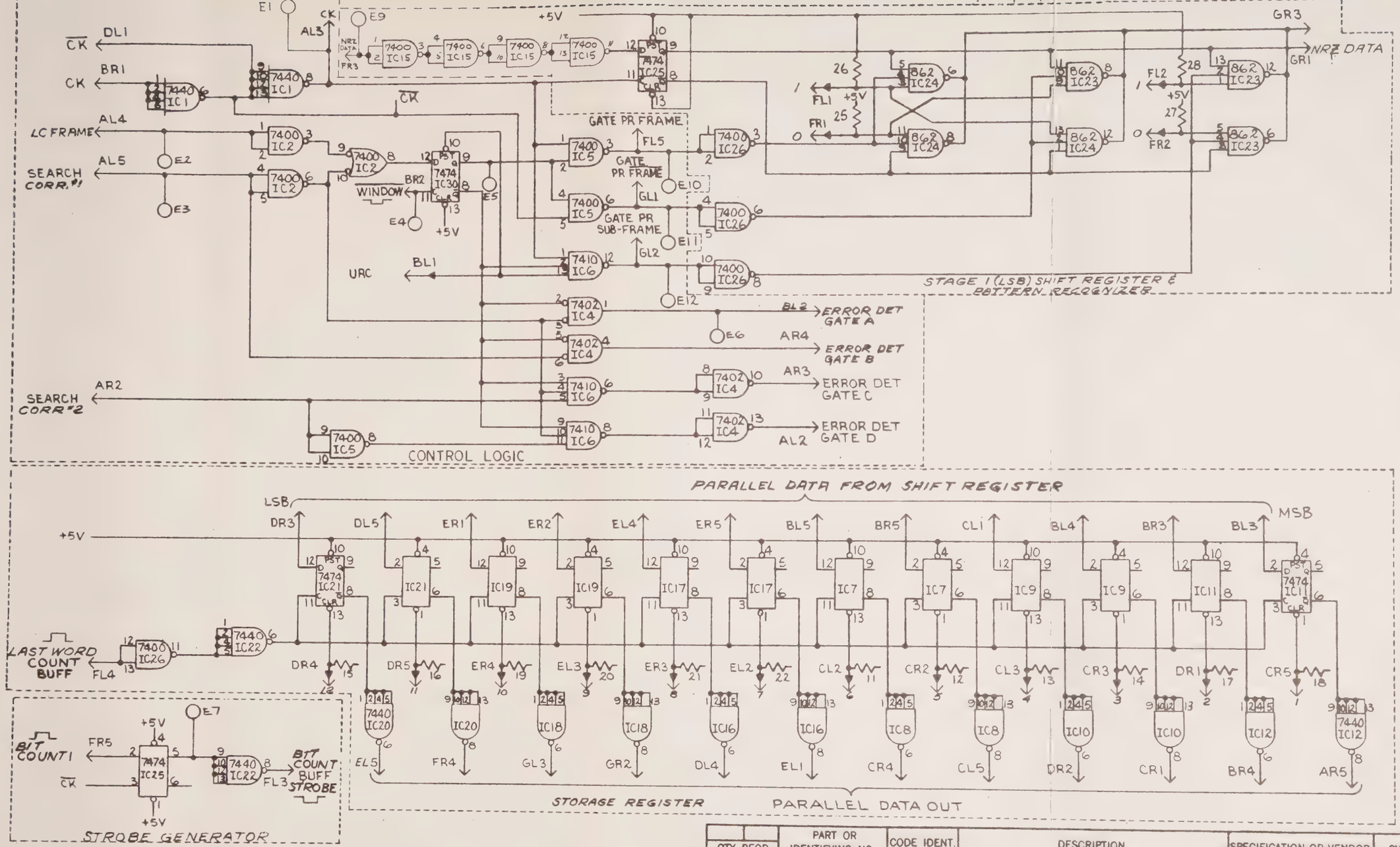
APPROVED
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y DATA STORAGE & CONTROL LOGIC

SIZE	CODE IDENT.	
D	08539	070057

SCALE —— SHEET ——



NOTES
1. SN7474 CONFIGURATION TYPICAL
2. ALL 7400'S PREFIXED BY SN & SUFFIXED BY N (EX. SN7440N)
3. ALL RESISTORS GO TO +5V.
4. ← INDICATES PROGRAMMABLE LINE

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
			LIST OF MATERIALS			

070057	
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.

		DATE
DRAWN	R. D. Edwardt	5-15-68
CHECKED		7/12/68
DESIGNER		
PROJECT ENG		7-17-68
APPROVED		

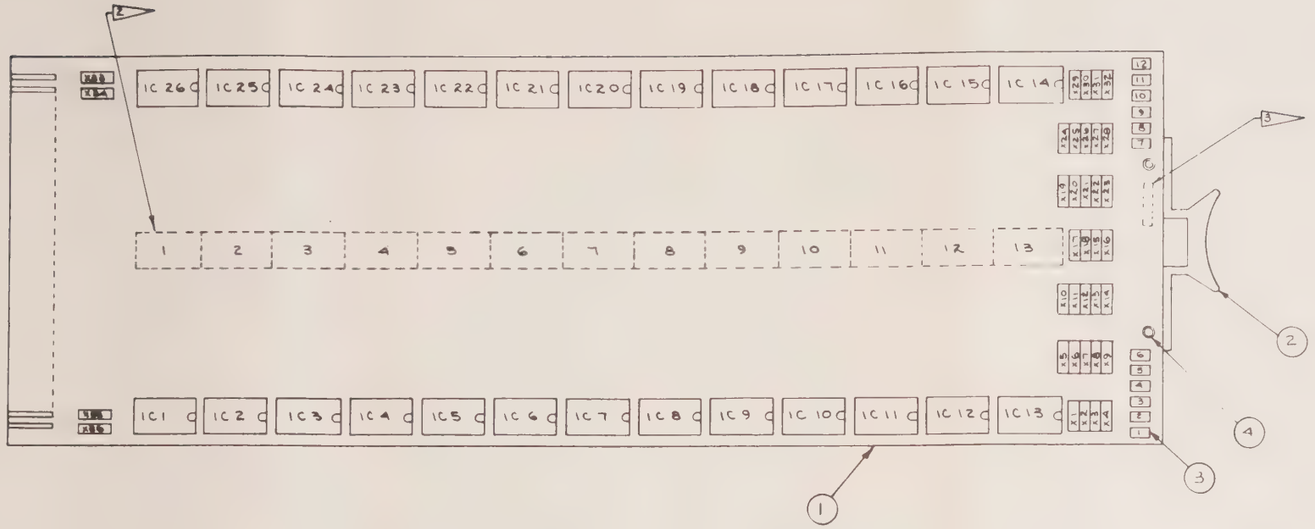
MATERIAL ±
FINISH ±
APPROVED
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC DATA STORAGE & CONTROL

SIZE	CODE IDENT.	
C	08539	075057

SCALE: ± E-259 SHEET ±



IC POS. CHART	
IC 1	SN7440N
2	SN7440N
3	SN7474N
4	SN15862N
5	
6	
7	SN15862N
8	SN7474N
9	SN15862N
10	
11	
12	SN15862N
13	
14	
15	
16	
17	SN7474N
18	SN15862N
19	
20	
21	SN15862N
22	SN7474N
23	SN15862N
24	
25	
IC 26	SN15862N

COMP POS. CHART	
X1	1K
X2	
X3	
X4	
X5	
X6	
X7	
X8	
X9	
X10	
X11	
X12	
X13	
X14	
X15	
X16	
X17	
X18	
X19	
X20	
X21	
X 22	
X 23	
X 24	
X 25	
X 26	
X 27	
X 28	
X 29	
X 30	
X 31	
X 32	1K
X 33	JUMP
X 34	.1UF 25V
X 35	.1UF 25V
X 36	JUMP

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE #070053REV
2. REPAIR PAD SECTIONS 1-13.
3. STAMP ASSEMBLY NO IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE #22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075053
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM 6 IN "A" HOLES.

ITEM	QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL
10	32	MS353508		RESISTOR 1/4W 10% 1K		
9	16	SN15862N		IC		
8	4	SN7474N		IC		
7	2	SN7440N		IC		
6	A/R	016467		CONNECTION PIN		
5	2	3C023		CAPACITOR .1UF 25V	SPRAGUE	
4	2	1200-5-02		RIVET	CTC	
3	12	8046-1		TEST JACK	AUGAT	E1-E12
2	1	SAE 6200		CARD PULL	STANFORD APPLIED	
1	1	079009		BOARD SUB-ASSY		

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
XXX ±N XX ±N
FRACTIONS ±N ANGLES ±N
FLATNESS WITHIN .
HOLE TOLERANCE PER D C S SPECIFICATION AS-81401B, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX
MATERIAL —N
FINISH —N

CONTRACT NO
DRAWN RG DATE 1-68
CHECKED RPW 2-68
DESIGNER
PROJECT ENG RG 1-68
APPROVED
APPROVED
APPROVED

NEXT ASSY | USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN

BOARD ASS'Y 8 BIT SHIFT REGISTER & PATTERN RECOGNIZER

SIZE D | CODE IDENT 08539 | 070053

SCALE —N | SHEET —N

PARALLEL DATA OUTPUTS

BL5 BR5 CL1 E10 CR4 DR3 DL5 ER1 FR3 E9

SERIAL DATA IN

BL2

E1 E6

AL3

$\overline{CK}$

7440 IC1

E5

E2

AL4

GATE PR FRAME

7440 IC1

E3

AL5

GATE PR FRAME

7440 IC2

E4

BR2

GATE PR SUB-FRAME

7440 IC2

7474 IC3

IC3 IC8 IC8 IC17 IC17 IC22 IC22

5V

AR2 AR4 BR1 BR4 BL3 CR1 CL3 CR3 DR4 DR5 ER3 EL2 FR1 FL1 GR3 GR1

1 2 5 6 9 10 13 14 15 16 21 22 25 26 29 30

862 IC4 862 IC4 862 IC6 862 IC6 862 IC9 862 IC9 862 IC11 862 IC11 862 IC18 862 IC18 862 IC20 862 IC20 862 IC23 862 IC23 862 IC25 862 IC25

E7

862 IC4 862 IC5 862 IC6 862 IC7 862 IC9 862 IC10 862 IC11 862 IC12 862 IC18 862 IC19 862 IC20 862 IC21 862 IC23 862 IC24 862 IC25 862 IC26

E11

AR3 AL2 BL4 BR3 CL2 CR2 DR1 CR5 ER4 EL3 ER2 FR4 FR2 FL2 GR2 GL3

3 4 7 8 11 12 17 18 19 20 23 24 27 28 31 32

862 IC5 862 IC5 862 IC7 862 IC7 862 IC10 862 IC10 862 IC12 862 IC12 862 IC19 862 IC19 862 IC21 862 IC21 862 IC24 862 IC24 862 IC26 862 IC26

E12

CL5 DR2 AR5 CL4 EL4 ER5 EL5 DL4

FRAME SYNC PATTERN

SUB FRAME SYNC PATTERN

TO ERROR DETECTOR

NOTES:

1. 7440 & 7474 ARE PREFIXED BY SN & SUFFIXED BY N (EX. SN7440N.).
2. 862 IS PREFIXED BY SN15 & SUFFIXED BY N.
3. ALL RESISTORS GO TO +5V.
4. ←— INDICATES PROGRAMMABLE LINE

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

070053

NEXT ASSY | USED ON

APPLICATION

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL

FINISH

CONTRACT NO.

DRAWN S.Q. Eckardt DATE 5-28-68

CHECKED J.K. BURLINSON 6-4-68

DESIGNER

PROJECT ENG P. Cannon 7-5-68

APPROVED

APPROVED

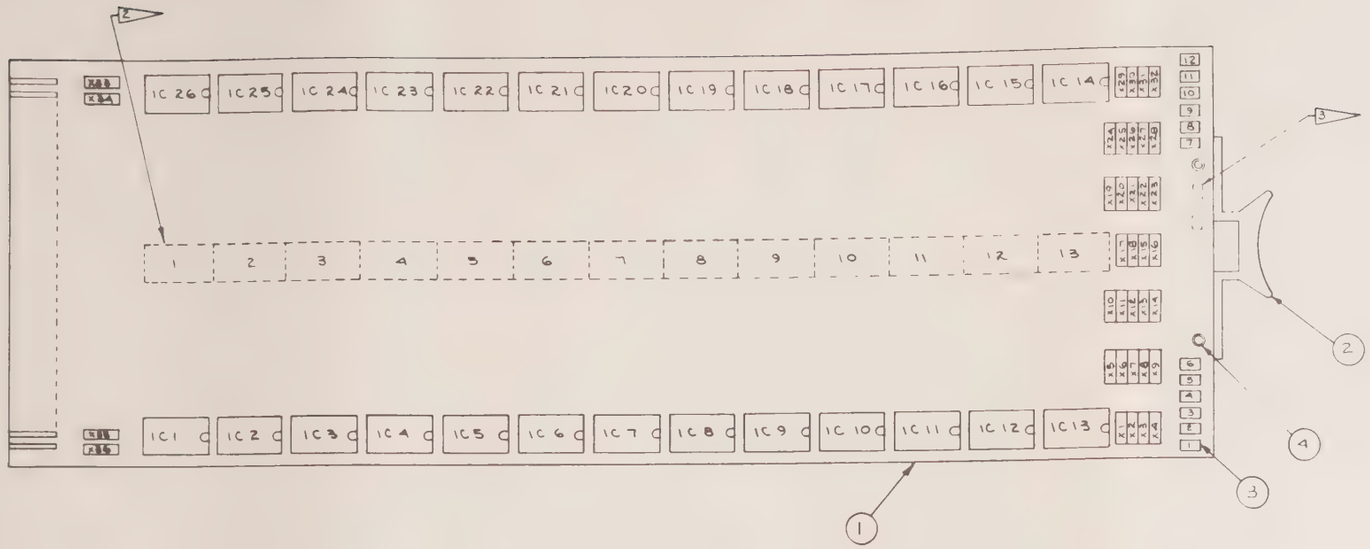
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC
8 BIT SHIFT REGISTER & PATTERN RECOGNIZER

SIZE C | CODE IDENT. 08539 | 075053

SCALE: | E259 | SHEET



IC POS. CHART	
IC 1	SN1583ON
2	SN7474N
3	SN7451N
4	SN7470N
5	↕
6	↕
7	SN7470N
8	SN7451N
9	SN7400N
10	——
11	SN1586ZN
12	SN7454N
13	SN7454N
14	SN7410N
15	SN7400N
16	SN7451N
17	SN7400N
18	SN7420N
19	SN7420N
20	SN7454N
21	SN7454N
22	SN7474N
23	SN7470N
24	↕
25	↕
IC 26	SN7470N

COMP POS. CHART	
X1	1K
X2	↕
X3	↕
X4	1K
X5	——
X6	1K
X7	↕
X8	
X9	
X10	
X11	
X12	↕
X13	1K
X14	——
X15	1K
X16	↕
X17	
X18	
X19	
X20	
X21	
X 22	
X 23	
X 24	↕
X 25	1K
X 26	1K
X 27	1K
X 28	1K
X 29	1K
X 30	1K
X 31	——
X 32	——
4 X 33	JUMP
X 34	.1UF 25V
X 35	.1UF 25V
4 X 36	JUMP

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE "070003REV
2. REPAIR PAD SECTIONS 1-13.
3. STAMP ASSEMBLY NR IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE "22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075003.
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM 6 IN "A" HOLES.

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
6 1	SN1586ZN		I.C.	T.I.		16
7 28	MS35350-8		RESISTOR 1/4W, 10%, 1K			15
2	SN7474N		I.C.	T.I.		14
1	SN1583ON		↕	↕		13
8	SN7470N					12
4	SN7454N					11
3	SN7451N					10
2	SN7420N					9
1	SN7410N		↕	↕		8
8	SN7400N		I.C.	T.I.		—
6 A/R	016467		CONNECTION PIN			6
2	3C023		CAPACITOR .1UF 25V	SPRAGUE		5
2	1200-5-02		RIVET	CTC		4
12	8046-1		TEST JACK	AUGAT	E1-E12	3
1	SAE 6200		CARD PULL	STANFORD APPLIED		2
1	079009		BOARD SUB-ASSY			1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
XXX —N— .XX —N—
FRACTIONS —N— ANGLES —N—
FLATNESS WITHIN —.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES. REMOVE BURRS .015 MAX

MATERIAL —N—

FINISH —N—

NEXT ASSY | USED ON

APPLICATION

CONTRACT NO.

		DATE
DRAWN	P. Gannon	2-7-68
CHECKED	RPW	2.7.68
DESIGNER		
PROJECT ENG.	P. Gannon	2-7-68
APPROVED		

APPROVED

APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y
BIT COUNTER & CODE CONVERTER

SIZE	CODE IDENT.	
D	08539	070003

SCALE —N— SHEET —N—

CODE CONVERTER

BIT COUNTER

NOTES:
1. SN7474N CONFIGURATION TYP.
2. ALL 7400'S PREFIXED BY SN & SUFFIXED BY N (EX. SN7440N)
3. ALL RESISTORS GO TO +5V.
4. ▶ INDICATES PROGRAMABLE LINE.

CODE CONVERTER PROGRAM

	A	B	C	D	E	
BI-Ø	1	0	1	1	0	1
BI-Ø	1	0	1	0	1	1
RZ	1	0	1	1	0	0
RZ	1	0	1	0	1	0
NRZL	0	0	0	1	0	0
NRZL	0	0	0	0	1	0
NRZM	0	1	1	1	0	0
NRZS	0	1	1	0	1	0

0=GRD
1=OPEN (+)

WINDOW PROG

	A	B
1 BIT	0	0
3 BIT	1	0
5 BIT	1	1

LIST OF MATERIALS

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.

DRAWN		DATE 5-17-68
CHECKED		7/15/68
DESIGNER		
PROJECT ENG		7-15-68
APPROVED		

MATERIAL

FINISH

APPROVED

APPROVED

070003 | NEXT ASSY | USED ON

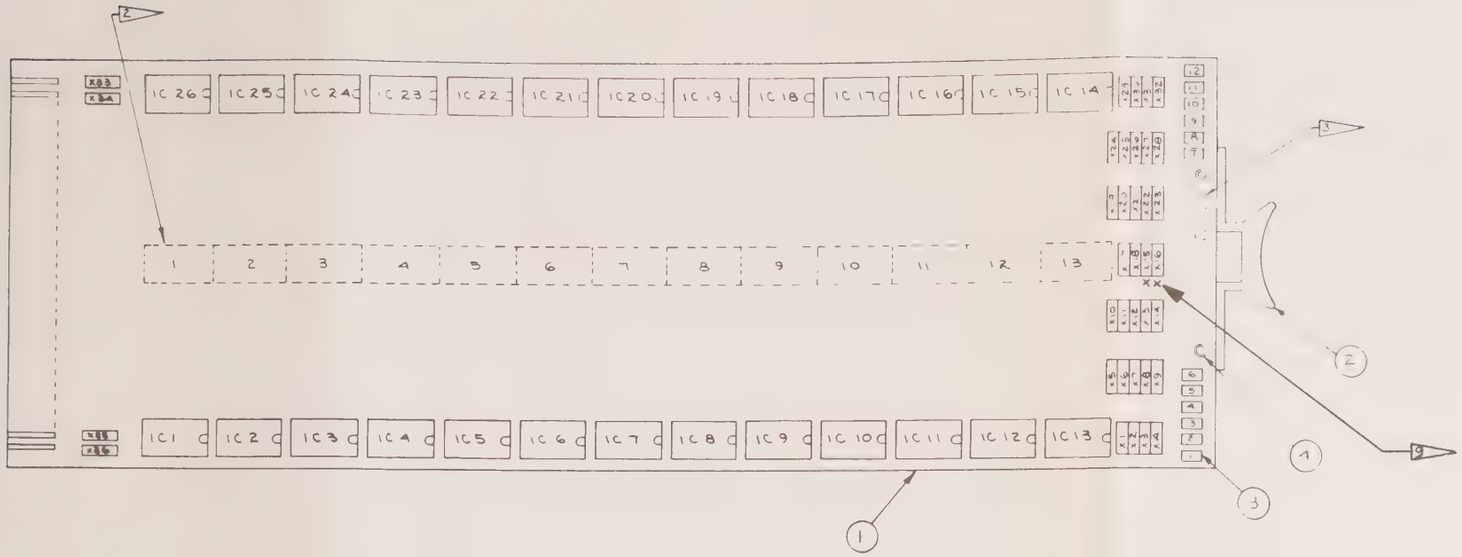
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC BIT COUNTER & CODE CONVERTER

SIZE	CODE IDENT.	
C	08539	075003

SCALE: | SHEET



IC POS. CHART	
IC 1	SN7410N
2	SN7400N
3	SN7400N
4	SN7440N
5	SN7474N
6	SN7451N
7	SN7400N
8	SN7474N
9	SN7474N
10	SN7474N
11	SN15846N
12	—
13	—
14	—
15	SN7402N
16	SN15846N
17	SN7400N
18	SN7470N
19	SN7451N
20	SN7400N
21	SN7474N
22	SN7470N
23	SN7474N
24	SN7474N
25	SN7454N
IC 26	SN7454N

COMP POS. CHART	
X1	—
X2	—
X3	—
X4	—
X5	—
X6	—
X7	—
X8	—
X9	—
X10	—
X11	—
X12	—
X13	1K
X14	1K
X15	—
X16	—
X17	1K
X18	1K
X19	—
X20	—
X21	—
X22	—
X23	—
X24	—
X25	—
X26	—
X27	—
X28	—
X29	—
X30	—
X31	—
X32	—
4 X33	JUMP
X34	.1UF 25V
4 X35	.1UF 25V
X36	JUMP

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE #070058 REV A
2. REPAIR PAD SECTIONS 1-13.
3. STAMP ASSEMBLY Nº IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE #22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075058
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM 6 IN "A" HOLES.
9. INSTALL FEED THRU IN COMP COMM BUSS FOR COMP 15 OR 16

ITEM	QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL
16	4	MS35350-8		RESISTOR 1/4W, 10% 1K		
15	2	SN15846N		IC	T.I.	
14	7	SN7474N		↕	↕	
13	2	SN7470N		↕	↕	
12	2	SN7454N		↕	↕	
11	2	SN7451N		↕	↕	
10	1	SN7440N		↕	↕	
9	1	SN7410N		↕	↕	
8	1	SN7402N		↓	↓	
7	5	SN7400N		IC	T.I.	
6	A/R	016467		CONNECTION PIN		
5	2	30023		CAPACITOR .1UF 25V	SPRAGUE	
4	2	1200-5-02		RIVET	CTC	
3	12	8046-1		TEST JACK	AUGAT	E1-E12
2	1	SAE 6200		CARD PULL	STANFORD APPLIED	
1	1	079009		BOARD SUB-ASSY		

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON
XXX —/— XX —/—
FRACTIONS —/— ANGLES —/—
FLATNESS WITHIN ⌒
HOLE TOLERANCE PER D C S SPECIFICATION AS-B14018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX
MATERIAL —/—
FINISH —/—

CONTRACT NO
DRAWN RG 1-68
CHECKED RPW 2-68
DESIGNER
PROJECT ENG RG 1-68
APPROVED
APPROVED
APPROVED

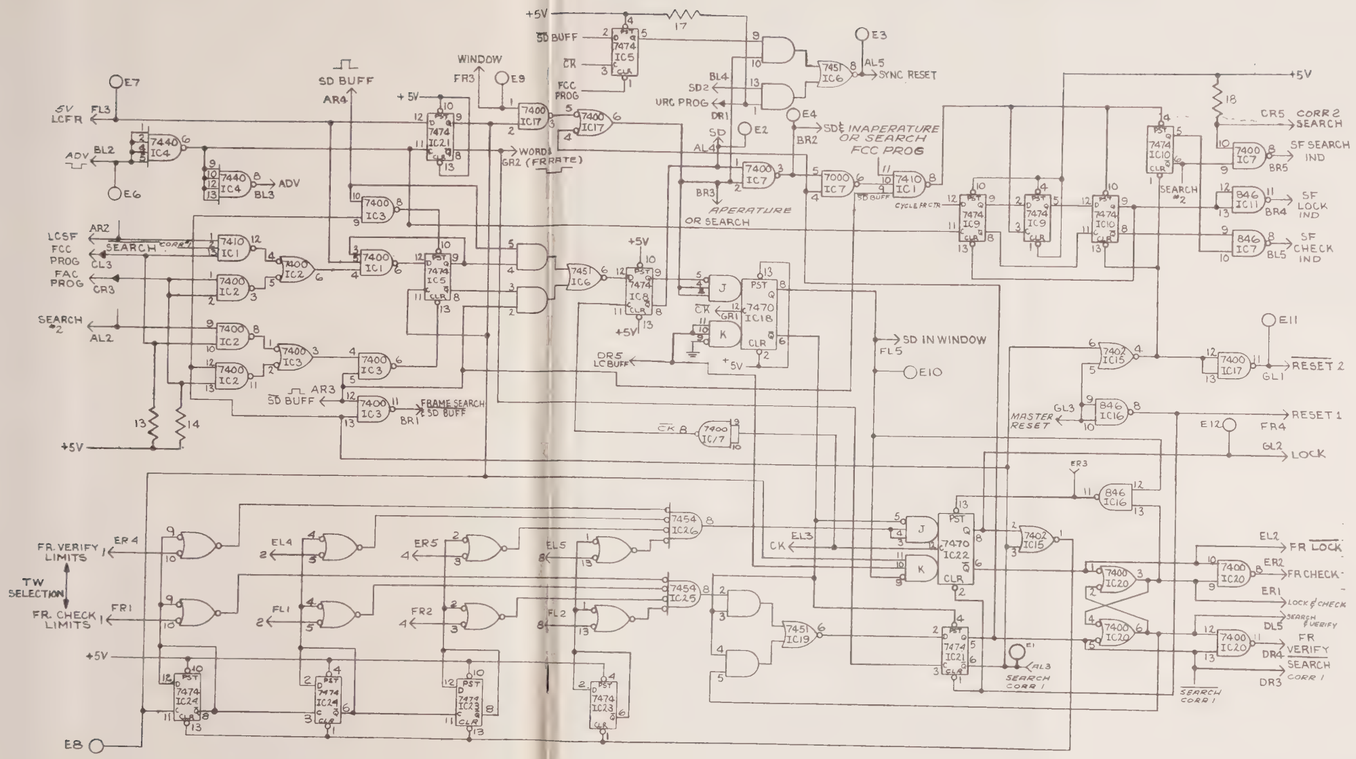
NEXT ASSY | USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y
CORRELATOR #1

SIZE D | CODE IDENT 08539 | 070058

SCALE —/— | E259 | SHEET —/—



NOTES:

1. ALL 7400'S ARE PREFIXED BY SN & SUFFIXED BY N. (EX. SN7400N).
2. 846 IS PREFIXED BY SN15 & SUFFIXED BY N.
3. ← INDICATES PROGRAM LINE

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN ⌒
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO

DRAWN — DATE 5-8-68
CHECKED
DESIGNER
PROJ ENG — DATE 7-15-68
APPROVED

MATERIAL ±
FINISH ±

APPROVED
APPROVED

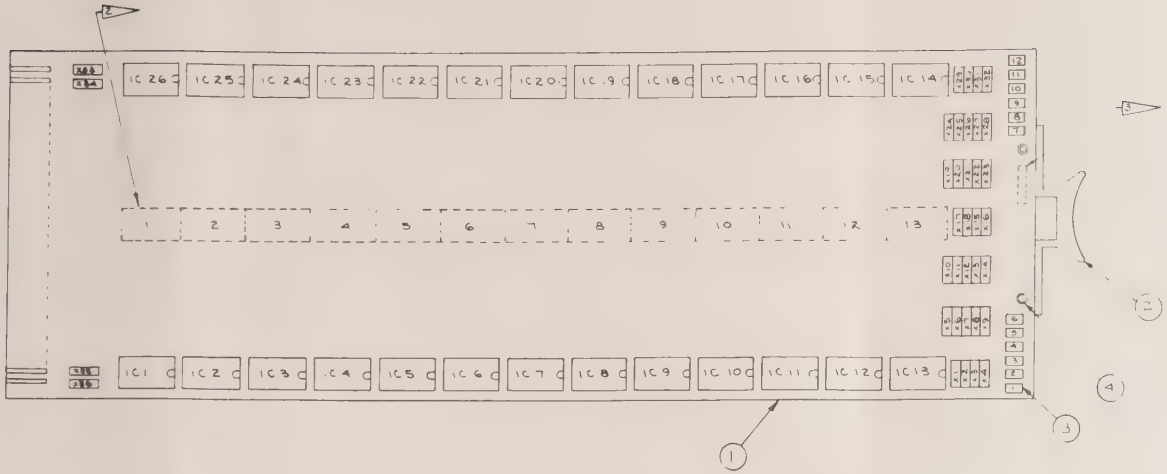
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC
CORRELATOR 1

070058	MULTIPLE
NEXT ASSY	USED ON
APPLICATION	

SIZE C | CODE IDENT. 08539 | 075058

SCALE ± | E259 | SHEET ±



IC POS. CHART	
IC 1	SN7400N
2	SN7400N
3	SN15846N
4	
5	
6	SN15846N
7	SN7474N
8	
9	
10	
11	SN7474N
12	SN7400N
13	SN7402N
14	—
15	—
16	—
17	SN7400N
18	SN7454N
19	SN7454N
20	SN7470N
21	SN7470N
22	SN7474N
23	SN7474N
24	SN7474N
25	SN7400N
IC 26	SN7400N

COMP POS. CHART	
X1	1K
X2	
X3	
X4	
X5	
X6	
X7	
X8	1K
X9	1K
X10	—
X11	1K
X12	—
X13	—
X14	—
X15	1K
X16	1K
X17	—
X18	1K
X 9	
X20	
X21	
X 22	
X 23	
X 24	
X 25	
X 26	
X 27	
X 28	1K
X 29	1K
X 30	1K
X 31	1K
X 32	1K
X 33	JUMP
X 34	.1UF 25V
X 35	.1UF 25V
X 36	JUMP

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE "070052REV C
2. REPAIR PAD SECTIONS 1-13
3. STAMP ASSEMBLY NR IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE "22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075052
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM 6 IN "A" HOLES.

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
27	MS35350X		RESISTOR 1/4W 10% 1K			13
1	SN7402N		IC			12
2	SN7470N		IC			11
2	SN7454N		IC			10
8	SN7474N		IC			9
4	SN15846N		IC			8
6	SN7400N		IC		T1	7
A/R	016467		CONNECTION PIN			6
2	3C023		CAPACITOR .1UF 25V	SPRAGUE		5
2	1200-5-02		RIVET	CTC		4
12	8046-1		TEST JACK	AUGAT		3
1	SAE 6200		CARD PULL	STANFORD APPLIED E-E		2
1	079009		BOARD SUB-ASSY			1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON
XXX — XX —
FRACTIONS — ANGLES —
FLATNESS W THIN —
HOLE TOLERANCE PER D C S SPECIFICATION AS-B1401B, CLASS 1
BREAK ALL CORNERS AND EDGES
REMOVE BURRS .015 MAX

MATERIAL —
FINISH —

NEXT ASSY | USED ON
APPLICATION

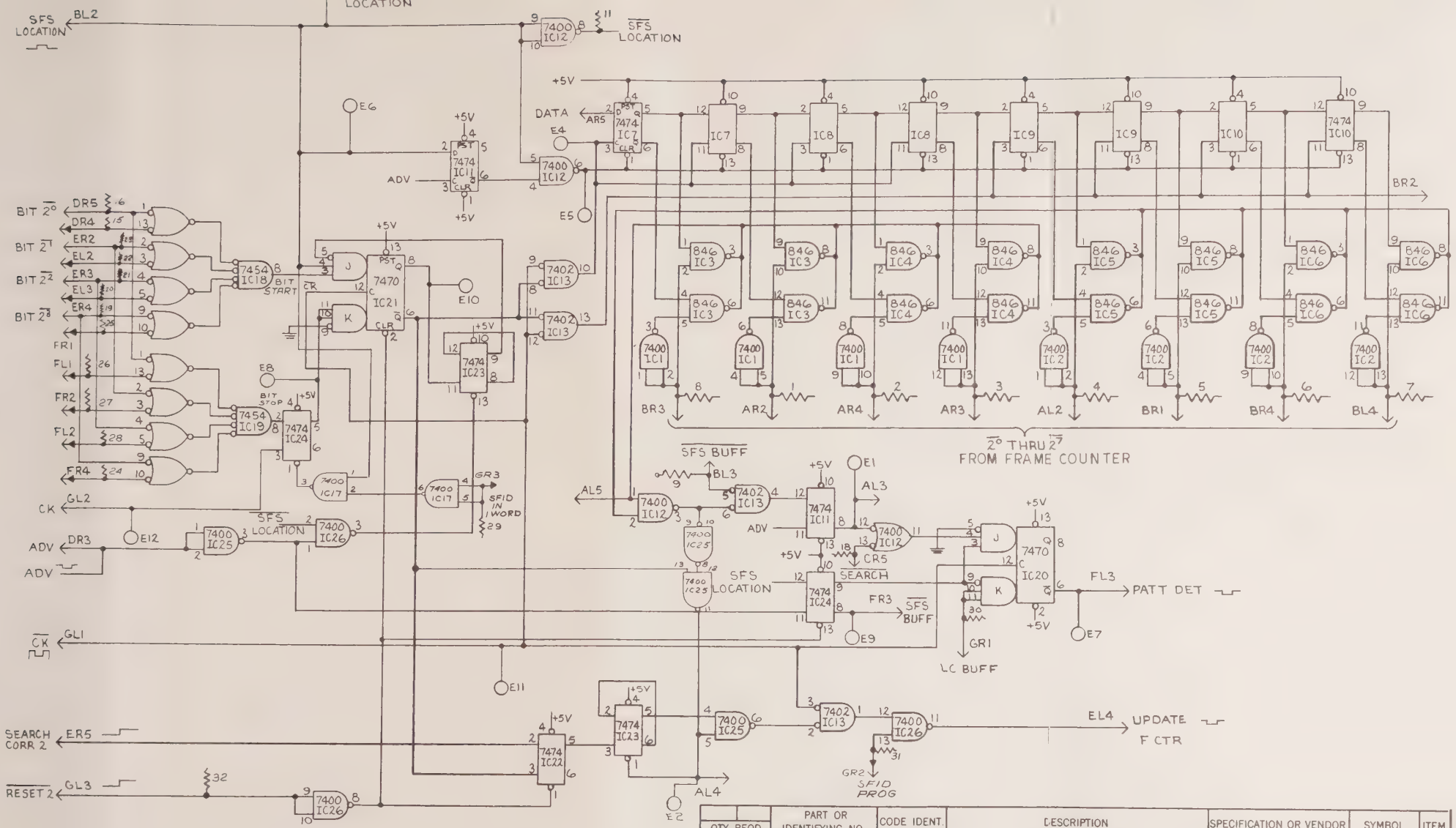
CONTRACT NO
DRAWN D.L. DATE 12-67
CHECKED R.F.I. 2-63
DESIGNER
PROJECT ENG R.G. 1-68
APPROVED
APPROVED
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y
SFID
SYNCHRONIZER

SIZE D | CODE IDENT 08539 | 070052

SCALE — | SHEET —



NOTES:

1. SN7474N CONFIGURATION TYP.
2. ALL 7400'S PREFIXED BY SN & SUFFIXED BY N (EX. SN7454N).
3. 846 IS PREFIXED BY SN15 & SUFFIXED BY N.
4. ALL RESISTORS GO TO +5V.
5. ← INDICATES PROGRAMMABLE LINE

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

070052	
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL ±

FINISH ±

CONTRACT NO.

		DATE
DRAWN	C. Eckardt	5-22-68
CHECKED	K. Burlinson	6-4-68
DESIGNER		
PROJECT ENG	R. Hammer	7-1-68
APPROVED		

APPROVED

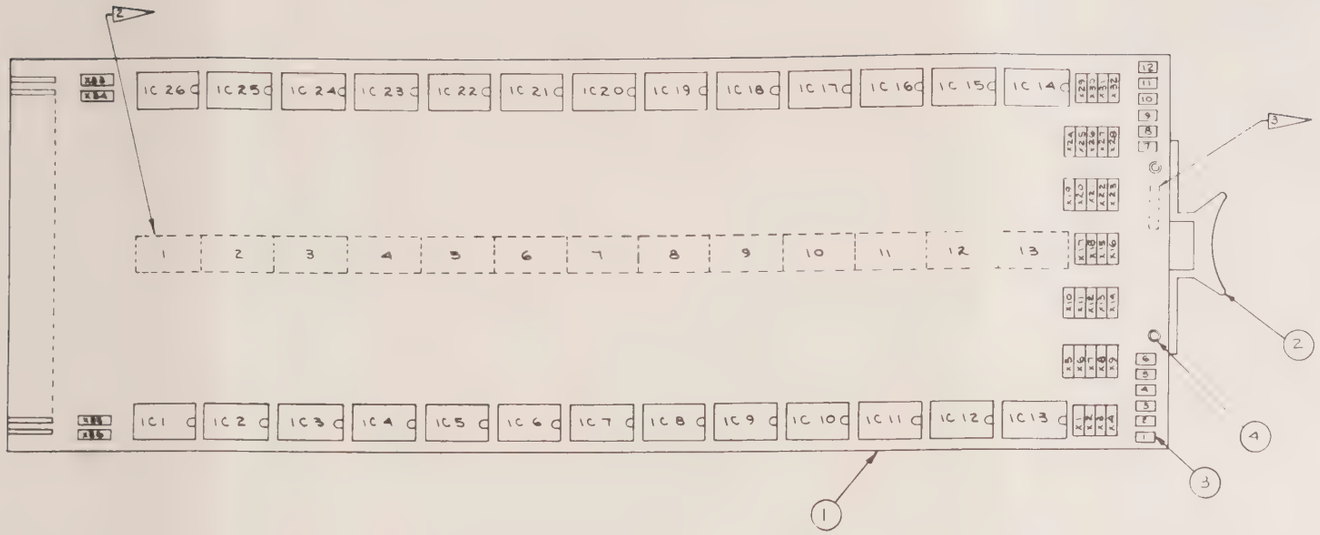
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC
SFID
SYNCHRONIZER

SIZE	CODE IDENT.	
C	08539	075052

SCALE: ± E259 SHEET ±



IC	POS.	CHART
IC	1	SN7470N
	2	SN7454N
	3	SN7454N
	4	SN7454N
	5	SN7410N
	6	SN7400N
	7	SN7402N
	8	SN7474N
	9	SN7470N
	10	SN7470N
	11	——
	12	——
	13	——
	14	——
	15	SN7400N
	16	SN7474N
	17	SN7400N
	18	SN7451N
	19	SN7402N
	20	SN7470N
	21	SN15846N
	22	SN7451N
	23	SN7474N
	24	SN7474N
	25	SN7454N
IC	26	SN7454N

COMP	POS	CHART
X1	——	
X2	——	
X3	——	
X4	1K	
X5	——	
X6	1K	
X7		
X8		
X9		
X10		
X11		
X12		
X13		
X14		
X15		
X16		
X17		
X18		
X19		
X20		
X21		
X22		
X23		
X24		
X25	1K	
X26	——	
X27	——	
X28	——	
X29	——	
X30	——	
X31	——	
X32	——	
4 X33	JUMP	
X34	.1UF 25V	
X35	.1UF 25V	
4 X36	JUMP	

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE #070059 REV B
2. REPAIR PAD SECTIONS 1-13.
3. STAMP ASSEMBLY NO IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE #22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075059.
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM 6 IN "A" HOLES.

ITEM	SYMBOL	SPECIFICATION OR VENDOR	DESCRIPTION	CODE IDENT.	PART OR IDENTIFYING NO.	QTY REQD
15			REGISTOR 1/4W, 10%, 1K		MS35350-8	21
14		T.I.	I.C		SN15846N	
13					SN7474N	4
12					SN7470N	4
11					SN7454N	5
10					SN7451N	2
9					SN7410N	1
8					SN7402N	2
7		T.I.	I.C.		SN7400N	3
6			CONNECTION PIN		016467	A/R
5		SPRAGUE	CAPACITOR .1UF 25V		3C023	2
4		CTC	RIVET		1200-5-02	2
3	E1-E12	AUGAT	TEST JACK		8046-1	12
2		STANFORD APPLIED	CARD PULL		SAE 6200	1
1			BOARD SUB-ASSY		079009	1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
XXX —/— XX —/—
FRACTIONS —/— ANGLES —/—
FLATNESS WITHIN —
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL —/—
FINISH —/—

CONTRACT NO.
DRAWN D Barrow DATE 1-31-68
CHECKED RJW 2-2-68
DESIGNER
PROJECT ENG. L Lemon 1-31-68
APPROVED
APPROVED
APPROVED

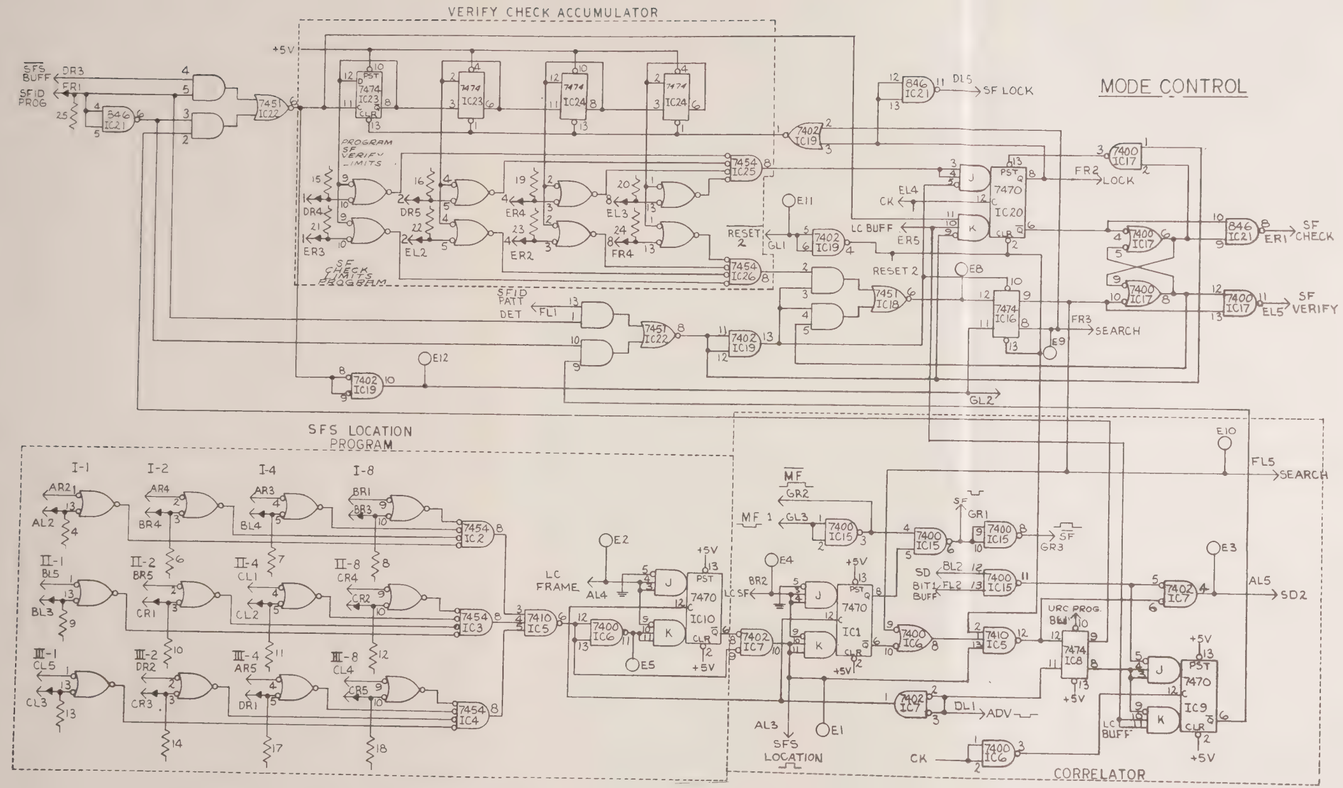
NEXT ASSY | USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y CORRELATOR #2

SIZE D | CODE IDENT 08539 | 070059

SCALE —/— SHEET —/—



NOTES:

1. SN7474N CONFIGURATION TYP.
2. ALL 7400'S PREFIXED BY SN & SUFFIXED BY N. (EX. SN7454N)
3. 846 IS PREFIXED BY SN16 & SUFFIXED BY N
4. ALL RESISTORS GO TO +5V.

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ± .005 .XX ± .01
FRACTIONS ± 1/64 ANGLES ± 1°
FLATNESS WITHIN ○
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.

DRAWN D. Q. Strandt DATE 5-23-68
CHECKED J. R. BURCINSON 6-9-68
DESIGNER
PROJECT ENG R. Lawrence 7-15-68
APPROVED

MATERIAL
APPROVED
FINISH
APPROVED

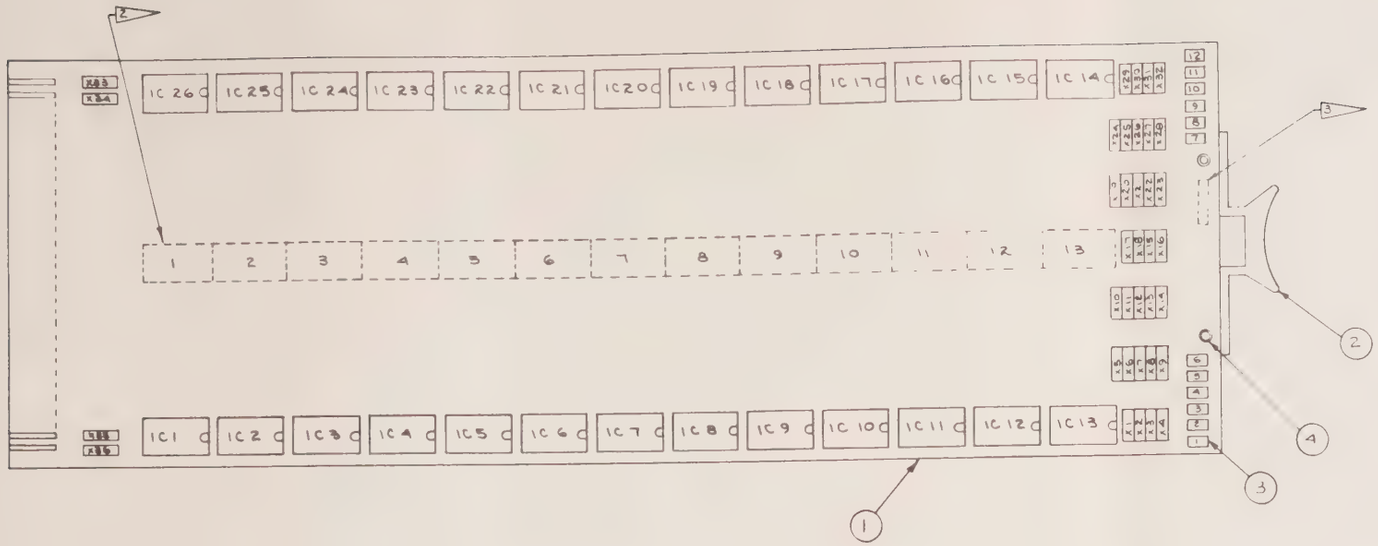
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC
CORRELATOR 2

075059

NEXT ASSY | USED ON
APPLICATION

SIZE C | CODE IDENT. 08539 | 075059
SCALE | E 259 | SHEET



IC POS. CHART	
IC 1	SN7470N
2	
3	
4	
5	
6	SN7470N
7	SN7400N
8	SN7400N
9	SN7410N
10	SN7410N
11	SN7454N
12	SN7454N
13	SN7402N
14	SN7454N
15	SN15846N
16	SN7410N
17	SN7410N
18	SN7410N
19	SN7400N
20	SN7400N
21	SN7470N
22	
23	
24	
25	
IC 26	SN7470N

COMP POS. CHART	
X1	1K
X2	
X3	
X4	
X5	
X6	
X7	
X8	
X9	
X10	1K
X11	
X12	
X13	
X14	
X15	1K
X16	1K
X17	1K
X18	
X19	1K
X20	
X21	
X 22	
X 23	
X 24	
X 25	
X 26	
X 27	
X 28	1K
X 29	
X 30	
X 31	
X 32	
X 33	JUMP
X 34	.1UF 25V
X 35	.1UF 25V
X 36	JUMP

NOTES:

1. DRILL MATRIX HOLES PER PAPER PUNCH TAPE #070047 REV A
2. REPAIR PAD SECTIONS 1-13.
3. STAMP ASSEMBLY Nº IN 3/32 HIGH CHARACTERS APPROX. AS SHOWN USING WHITE INDELIBLE INK.
4. USE #22 AWG SOLID WIRE.
5. FOR LOGIC SEE 075047.
6. SEE IC POSITION CHART.
7. SEE COMP. POSITION CHART.
8. INSTALL ITEM #6 IN "A" HOLES.

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
23	MS353508		RESISTOR 1/4W, 10% 1K			13
1	SN15846N		I C.	TI		12
12	SN7470N					11
3	SN7454N					10
5	SN7410N					9
1	SN7402N					8
4	SN7400N		I. C	TI		7
A/R	016467		CONNECTION PIN			6
2	3C023		CAPACITOR .1UF 25V	SPRAGUE		5
2	1200-3-02		RIVET	CTC		4
12	8046-1		TEST JACK	AUGAT	E1-E12	3
1	SAE 6200		CARD PULL	STANFORD APPLIED		2
1	079009		BOARD SUB-ASSY			1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON
XXX ±.010 XX ±.02
FRACTIONS ±1/64 ANGLES ±1°
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.
DRAWN RG DATE 1-68
CHECKED RPW 2 68
DESIGNER
PROJECT ENG RG 1-68
APPROVED

MATERIAL
FINISH

APPROVED
APPROVED

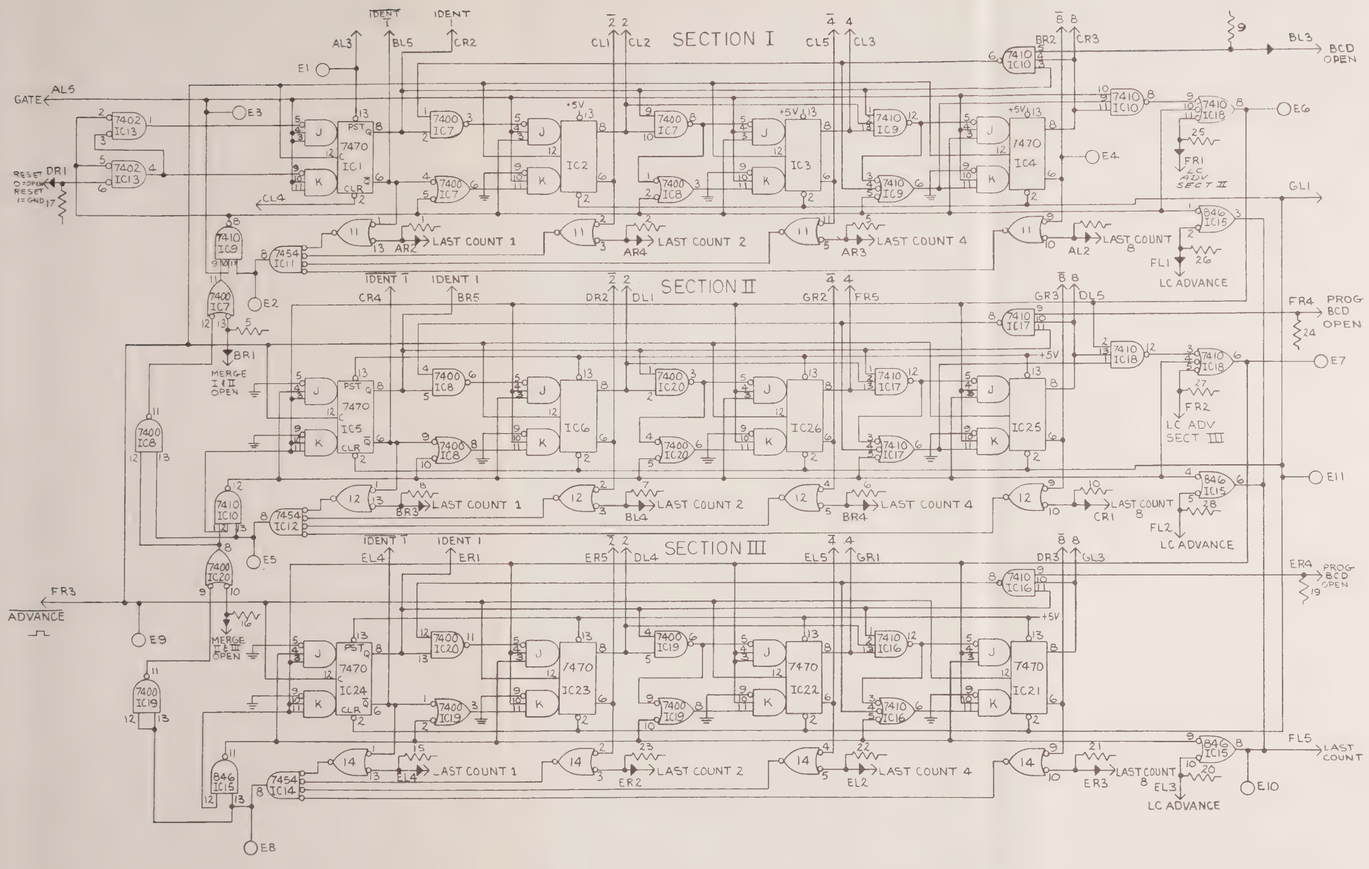
NEXT ASSY | USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y FORMAT COUNTER

SIZE D | CODE IDENT 08539 | 070047

SCALE | SHEET



NOTES:

1. ALL 7400'S PREFIXED BY SN & SUFFIXED BY N (EX. SN7454N).
2. 846 IS PREFIXED BY SN15 & SUFFIXED BY N.
3. ALL RESISTORS GO TO +5V
4. ⊣▸ INDICATES PROGRAMABLE LINE

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD B
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ± .XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION A5-B1401B, CLASS 1
BREAK ALL CORNERS AND EDGES. REMOVE BURRS .015 MAX

CONTRACT NO.

DRAWN S.D. Eckardt DATE 5-27-68
CHECKED S.K. Swenson 6-9-68
DESIGNER
PROJECT ENG. 7-15-68
APPROVED

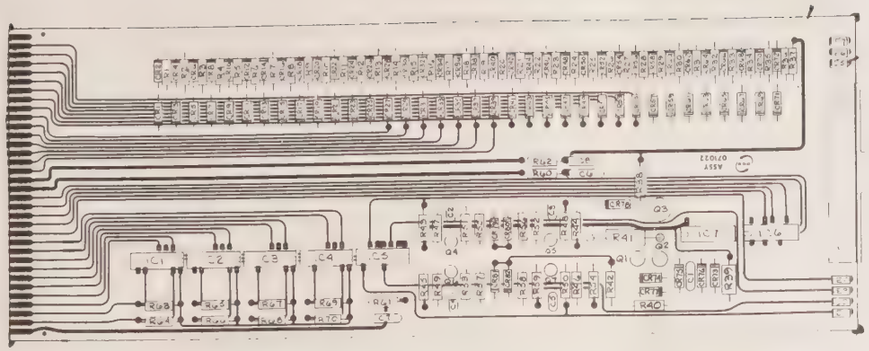
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

LOGIC FORMAT COUNTER

MATERIAL
APPROVED
FINISH
APPROVED

075047
NEXT ASSY | USED ON
APPLICATION

SIZE C | CODE IDENT. 08539 | 075047
SCALE | E 259 | SHEET



NOTES

1. ASSEMBLE PER DCS WORKMANSHIP MANUAL QS 5000 SERIES
2. AFFIX ITEM 28 UNDER ITEMS 21
3. AFFIX ITEM 29 UNDER ITEM 22.
4. FOR SCHEMATIC SEE DWG. 071083
5. COMPONENTS NOT TO EXCEED 5/16 IN HEIGHT

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
7	8046-1		TEST JACK	AUGAT	E1-E7	32
2	1200-5-02		RIVET	CTC		31
1	6200		HANDLE	S.A.E.		30
1	294-296-T		TRANSIPAD	MANADOCK		29
2	A10042		TRANSIPAD	ROSS		28
1	SN7440N		INTEGRATED CIRCUIT	TI	IC7	27
1	SN7474N		↓ ↓	↓	IC6	26
1	SN7400N		↓ ↓	↓	IC5	25
4	SN7454N		INTEGRATED CIRCUIT	TI	IC1-IC4	24
4	2N3640		TRANSISTOR		Q4-Q7	23
1	2N8133		TRANSISTOR		Q3	22
2	2N3227		TRANSISTOR		Q1&Q2	21
2	IN816		DIODE		CR77&CR78	20
2	CER 69		DIODE		CR75&CR76	19
78	IN3067		DIODE		CR1-CR74 CR79&CR82	18
1	BWH		RESISTOR 2W 5% 390Ω	IRC	R41	17
1	MS35043-20		½W 10% 1.5K		R40	16
1	MS35043-11		½W 470Ω		R39	15
1	MS35043-16		½W 3.3K		R38	14
1	TYPE CB		¼W 2.7Ω	ALLEN-BRADLEY	R61	13
2	TYPE CB		10% 5.6Ω	ALLEN-BRADLEY	R60&R62	12
4	MS35350-110		5% 15K		R51-R54	11
4	MS35350-87		5% 1.6K		R47-R50	10
12	MS35350-8		10% 1K		R43 R46 & R63 R70	9
3	MF5C-D		1% 5.11K	ELECTRA	R57-R59	8
1	↓		10.2K	↓	R56	7
1	↓		14.3K	↓	R42	6
38	MF5C-D		RESISTOR ¼W 1% 20.5K	ELECTRA	R1-R37&R55	5
2	5C023474X0250B3		CAPACITOR 25V, 20%, .47UF	SPRAGUE	C6&C8	4
4	DM10-100K		CAPACITOR 10% 10PF	ARCO	C2-C5	3
2	3C023104X0250A3		CAPACITOR 25V, 20% .1UF	SPRAGUE	C1&C7	2
1	071021		BOARD SUB-ASS'Y			1
-1	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON: .XXX ±.010 .XX ±.02
FRACTIONS ±1/64 ANGLES ±1°
FLATNESS WITHIN .003
HOLE TOLERANCE PER D C S SPECIFICATION AS 814018, CLASS 1
BREAK ALL CORNERS AND EDGES. REMOVE BURRS .015 MAX

CONTRACT NO
DRAWN J. Anderson DATE 5-22-68
CHECKED J. R. Brunson 5-23-68
DESIGNER Ronald Martin 5-28-68
PROJECT ENG
APPROVED
MATERIAL
APPROVED
FINISH
APPROVED

FINAL | MULTIPLE
NEXT ASSY | USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASS'Y
ERROR DETECTOR

SIZE D | CODE IDENT 08539 | 071022
SCALE: FULL | E 259 | SHEET

-24V IN ← DL2
+24V IN ← DL3
+5V IN ← AL1
CURRENT SUM ← GR3

CR1-CR72 IN3067

R1-R36 20.5K 1%

PR1 ← ER4 CR1 CR2 → R1
PR2 ← ER3 CR3 CR4 → R2
PR3 ← ER2 CR5 CR6 → R3
PR4 ← ER1 CR7 CR8 → R4
PR5 ← DR5 CR9 CR10 → R5
PR6 ← DR4 CR11 CR12 → R6
PR7 ← DR3 CR13 CR14 → R7
PR8 ← DR2 CR15 CR16 → R8
PR9 ← DR1 CR17 CR18 → R9
PR10 ← CR5 CR19 CR20 → R10
PR11 ← CR4 CR21 CR22 → R11
PR12 ← CR3 CR23 CR24 → R12
PR13 ← CR2 CR25 CR26 → R13
PR14 ← EL5 CR27 CR28 → R14
PR15 ← EL4 CR29 CR30 → R15
PR16 ← EL3 CR31 CR32 → R16
PR17 ← EL2 CR33 CR34 → R17
PR18 ← EL1 CR35 CR36 → R18
PR19 ← DL5 CR37 CR38 → R19
PR20 ← DL4 CR39 CR40 → R20
PR21 ← FL1 CR41 CR42 → R21
PR22 ← FL2 CR43 CR44 → R22
PR23 ← FL3 CR45 CR46 → R23
PR24 ← FL4 CR47 CR48 → R24
PR25 ← FL5 CR49 CR50 → R25
PR26 ← GL1 CR51 CR52 → R26
PR27 ← GL2 CR53 CR54 → R27
PR28 ← GL3 CR55 CR56 → R28
PR29 ← ER5 CR57 CR58 → R29
PR30 ← FR1 CR59 CR60 → R30
PR31 ← FR2 CR61 CR62 → R31
PR32 ← FR3 CR63 CR64 → R32
PR33 ← FR4 CR65 CR66 → R33
PR34 ← FR5 CR67 CR68 → R34
PR35 ← GR1 CR69 CR70 → R35
PR36 ← GR2 CR71 CR72 → R36

R61 2.7Ω
R62 5.6Ω
R60 5.6Ω
C7 .1 UF
C8 .47UF
C6 .47UF

R38 3.3K 1/2W
Q3 2N3133
CR78 IN816
R37 20.5K 1%

R39 470Ω 1/2W
R40 1.5K 1/2W
R41 390Ω 2W
Q1 2N3227
Q2
CR75 CER 69
CR76
C1 .1UF
CR74 IN3067
CR73 IN3067
CR77 IN3067

CR79 IN3067
CR80 IN3067
CR81 IN3067
CR82 IN3067

Q4 2N3640
Q5 2N3640
Q6 2N3640
Q7 2N3640

R42 14.3K 1%
R43 1K
C2 10PF
R47 1.6K 5%
R51 15K 5%
R55 20.5K 1%
R44 1K
C3 10PF
R48 1.6K 5%
R52 15K 5%
R56 10.2K 1%
R45 1K
C4 10PF
R49 1.6K 5%
R53 15K 5%
R57 5.11K 1%
R46 1K
C5 10PF
R50 1.6K 5%
R54 15K 5%
R58 5.11K 1%
R59 5.11K 1%

IC7 SN7440N
IC6 SN7474N

CL3 → CLOCK
CL4 → SYNC DET BUFF
DL1 → SYNC DET BUFF
CL2 → ED OUT
CL5 → CLOCK

E1 E2 E3 E4 E5 E6 E7

AL2 AL3 AR2 AR3 AR4 BR1 AR5 BR2 BR8

R64 1K
R63 1K
R66 1K
R65 1K
R68 1K
R67 1K
R70 1K
R69 1K

IC1 SN7454N
IC2 SN7454N
IC3 SN7454N
IC4 SN7454N
IC5 SN7400N

AR1 → GRD.
BR4
BR5
CR1

AL5 AL4 BL2 BL1 BL4 BL3 CL1 BL5

NOTES:
1. ALL RESISTORS ARE 1/4W UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE 10% UNLESS OTHERWISE SPECIFIED.

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ±.010 .XX ±.02
FRACTIONS ±1/64 ANGLES ±1°
FLATNESS WITHIN .001
HOLE TOLERANCE PER D.C.S. SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL
FINISH

CONTRACT NO
DRAWN T. Anderson DATE 5-22-68
CHECKED J.R. Burlingson 5-23-68
ENGINEER [illegible] 5-29-68
PROJECT ENG
APPROVED
APPROVED
APPROVED

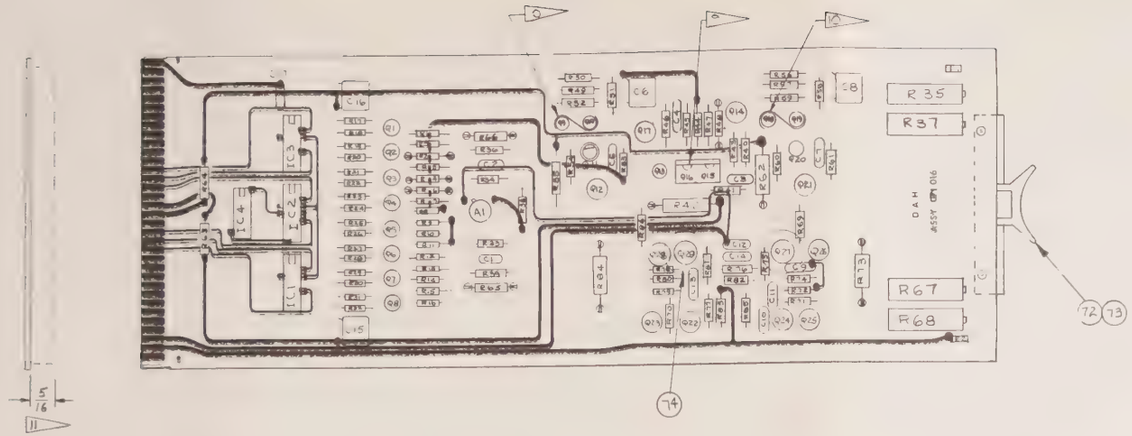
071022
NEXT ASSY USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

SCHEMATIC
ERROR DETECTOR BD.

SIZE D | CODE IDENT 08539 | 071035

SCALE ——— | E239 | SHEET ———



NOTES:

1. ASSEMBLE PER DCS WORKMANSHIP MANUAL AS 832011-5000.

2 > SYMBOLS FOR ITEM 59: R18, R20, R22, R24 R26, R28, R30 & R32.

3 > SYMBOLS FOR ITEM 37: R17, R19, R21, R23, R25, R27, R29, R31, R75 & R82

4. FOR SCHEMATIC SEE DWG. 071031.

6 > INSTALL ITEM 65 UNDER: Q27, Q29, Q21, Q17, Q4 & Q2

7 > INSTALL ITEM 66 UNDER: Q25, Q24, Q19, Q18, Q10 & Q9

9 > CLAMP ITEM 71 OVER Q15 & Q16 (ITEM 60) BEFORE INSERTING INTO ITEM 1.

10 > INSTALL Q9 & Q10, Q18 & 19 (ITEM 75) & ITEM 66 INTO BOARD, THEN INSTALL ITEM 70 & GLUE (ITEM 55), THEN SOLDER.

11 > COMPONENTS NOT TO EXCEED 5/16 IN HEIGHT

QTY	PART NO	DESCRIPTION	VENDOR	SYMBOL	ITEM
1	AS821021	TRANSISTOR MATCHED PAIR		Q15 & Q16	78
1	AS821009	TRANSISTOR MATCHED PAIR		Q24 & Q25	77
1	CA3015	AMPLIFIER	RCA	A1	76
2	AS821010	TRANSISTOR MATCHED PAIR		Q9, Q10 Q18 & Q19	75
2	TX8F-032-025B	HEAT SINK	IERC		74
2	1200-5-02	RIVET	CTC		73
1	6200	HANDLE	S.A.E.		72
1	31208	THERMAL CLAMP			71
2	259-.4	THERMAL EQUALIZING LINK	WAKEFIELD		70
1	SN15830N	INTEGRATED CIRCUIT	T.I.	IC4	69
3	SN7475N	INTEGRATED CIRCUIT	T.I.	IC1-IC3	68
2	80460-1	TEST JACK	AUGAT	E1 & E2	67
6	A10042	TRANSIPAD	MILTON ROSS		66
6	294-296-T	TRANSIPAD	MANADOC		65
2	2N4237	TRANSISTOR		Q21 & Q29	64
1	AS821018	MATCHED PAIR		Q22 & Q23	63
1	TN53			Q17	62
3	2N3638			Q12, Q14 & Q21	61
5	2N3856A			Q11, Q20 & Q26	60
2	2N4250			Q13 & Q28	59
8	2N3640	TRANSISTOR		Q1-Q8	58
1	3012P-1-103	POTENTIOMETER 10K	BOURNS	R67	57
3	3012P-1-501	POTENTIOMETER 500Ω	BOURNS	R35, R37, R82	56
A/R		EPOXY, GLUE			55

QTY REQD	PART OR IDENTIFYING NO	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
2	MFSC-D		RESISTOR 1/4W 1% F.A.	ELECTRA	R65 & R66	54
2	BWH		2W 5% 100Ω	IRC	R73 & R84	53
1	MS353350-157		1/4W 5% 130 MEG		R15	52
1	BWH		2W 5% 150Ω	IRC	R42	51
1	MS35044-9		2W 10% 220Ω		R62	50
1	MS35043-5		1/2W 470Ω		R55	49
2	MS35043-1		1/2W 10Ω		R76 & R81	48
1	MS35043-207		1/2W 3.9K		R38	47
4			1/4W 267Ω	ALLEN-BRADLY	R63, R64, R86	46
1	MS353350-12		4.7K		R51	45
3	-208		5.6K		R50, R57 & R58	44
3	-8		1K		R46, R53 & R61	43
1	-206		2.7K		R43	42
3	-202		560Ω		R41, R54 & R60	41
1	-15		15K		R40	40
8	-20		100K		2 >	39
2	-4		220Ω		R33 & R34	38
10	-13		6.8K		3 >	37
5	MS353350-214		10% 56K		R9, R10, R12, R14 & R16	36
1	MF5C-D		1% 909Ω	ELECTRA	R85	35
1			2.80K		R83	34
1			26.1K		R80	33
1			1.21K		R79	32
1			2.31K		R78	31
1			23.7K		R77	30
1			14.7K		R74	29
1			8.87K		R72	28
1			17.8K		R70	27
1			4.22K		R71	26
1			7.50K		R52	25
1			12.1K		R49, R56 & R59	24
1			7.15K		R44	23
1			5.11K		R45	22
1			FA		R48	21
1			2.87K		R47	20
1			3.74K		R39	19
1			1.69K		R36	18
1			6.98K		R13	17
1			348K		R11	16
1			174K		R9	15
1			82.5K		R7	14
1			FA		R6	13
1			42.2K		R5	12
1			FA		R4	11
1			21.5K		R3	10
1			FA		R2	9
1	MF5C-D		RESISTOR 1/4W 1% 11.0K	ELECTRA	R1	8
1	DM-10-220-K		CAPACITOR 22PF 100V 20%	ARCO	C10	7
4	5092-5474-X05-Q83		.47UF 50V	SPRAGUE	C13, C9, C12 & C16	6
1	3C023104X0250B3		.1 UF 25V 20%	SPRAGUE	C17	5
3	5C23105X0250B3		1.0UF 25V	SPRAGUE	C4, C6 & C8	4
6	TYPE TA		.01UF 100V	RMC	C3, C5, C7, C11, C12 & C14	3
2	DM-10-680F		CAPACITOR 68PF 100V	ARCO	C1 & C2	2
1	071015		BOARD DETAIL			1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MANUFACTURER
UNLESS OTHERWISE SPECIFIED TOLERANCES ON
XXX ± XX ±
FRACTIONS ± ANGLES ±
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS 81401B, CLASS 1
BREAK ALL CORNERS AND EDGES.
REMOVE BURRS .015 MAX

CONTRACT NO
DRAWN RPW DATE 12-4-67
CHECKED R. Burlington 1-22-68
DESIGNED R. Burlington 1-22-68
PROJECTED Robert M. Cole 2-12-68
APPROVED [signature] 2-19-68
MATERIAL
APPROVED
FINISH
APPROVED

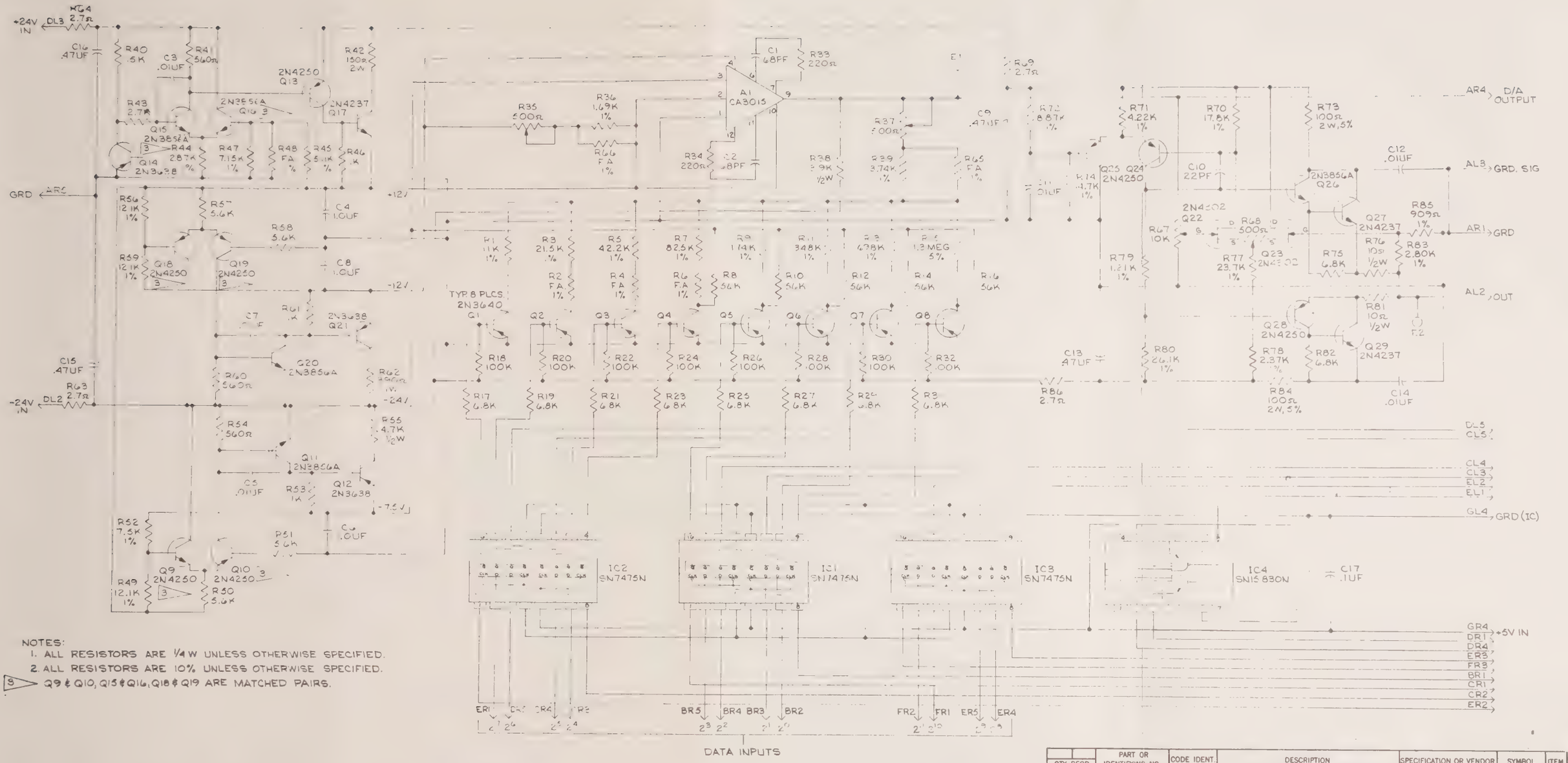
DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASSEMBLY
DA-H

FINAL	MULTIPLE
NEXT ASSY	USED ON
APPLICATION	

SIZE	CODE IDENT	
D	08539	071016

SCALE NONE E259 SHEET



NOTES:
1. ALL RESISTORS ARE 1/4 W UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE 10% UNLESS OTHERWISE SPECIFIED.
3. Q9 & Q10, Q15 & Q16, Q18 & Q19 ARE MATCHED PAIRS.

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON
XXX ±
XX ±
FRACTIONS ±
ANGLES ±
FLATNESS WITHIN
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES
REMOVE BURRS .015 MAX

CONTRACT NO.
DRAWN — DATE 5-6-6[illegible]
CHECKED — 5-23-6[illegible]
DESIGNER — 5-23-6[illegible]
PROJECT ENG
APPROVED

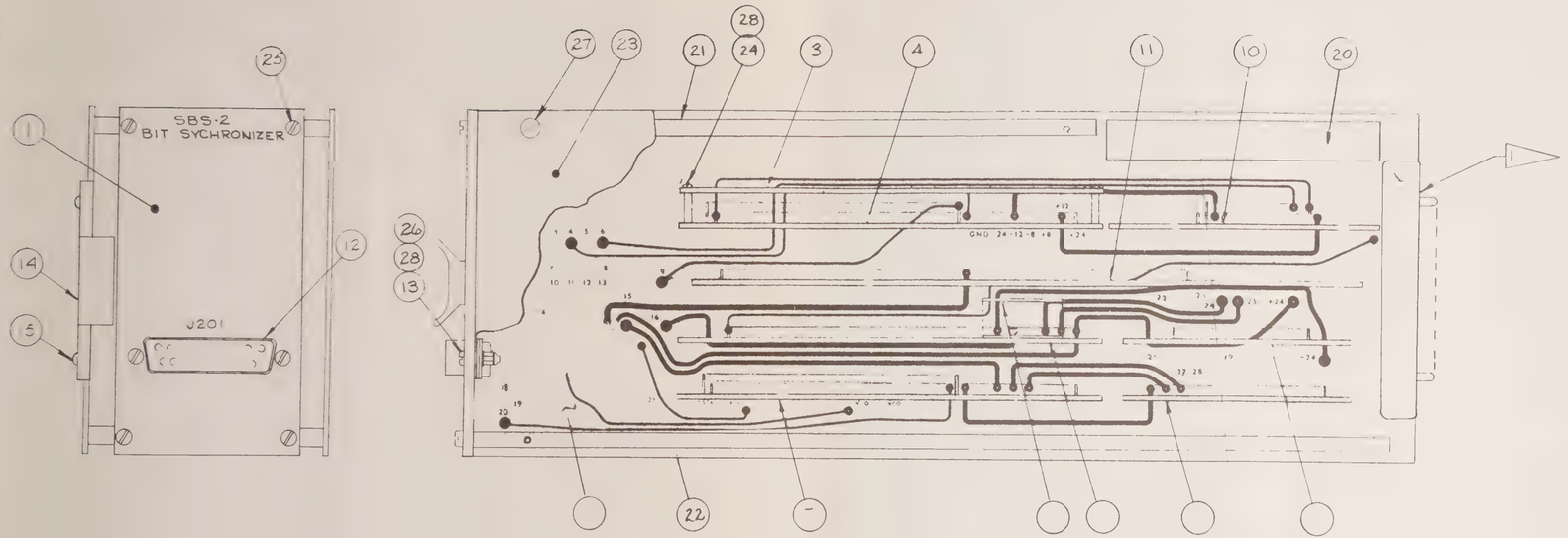
MATERIAL
FINISH
APPROVED
APPROVED

071016
NEXT ASSY | USED ON
APPLICATION

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

SCHEMATIC
D/A-H BD.

SIZE D | CODE IDENT. 08539 | 071031
SCALE | E 259 | SHEET



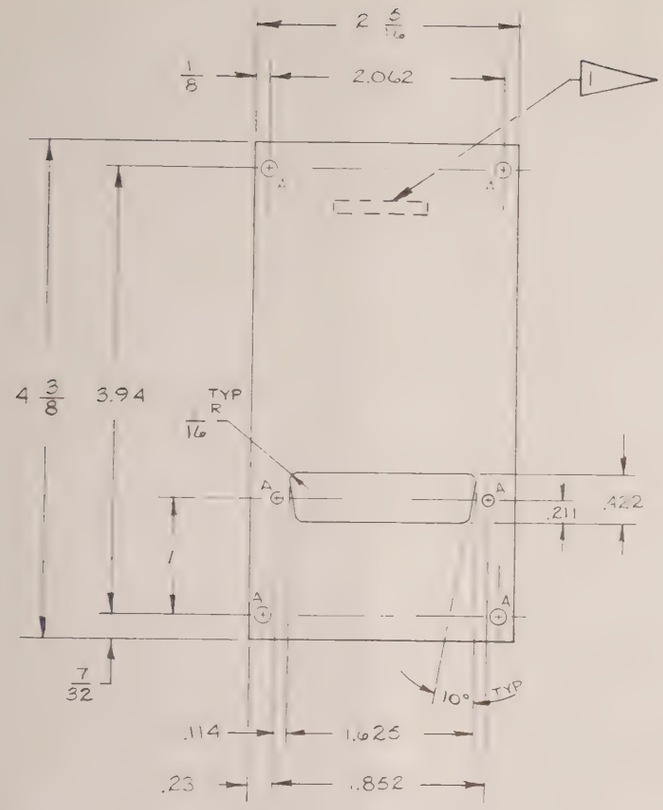
A/R	GRADE C (4-1)		LOCTITE	LOCTITE CORP.		
4			WASHER, FLAT #2	CPS		
17			SCREW, PH 4-40 x 3/16 SLOTTED			
2			2-56 x 1/2			
4			2-56 x 3/8			
4			SCREW, PH 2-56 x 1/4 SLOTTED	CPS		
1	755371		COVER PLATE			
1	756332-1		SUPPORT, BOTTOM			
1	756332-2		SUPPORT, TOP			
1	755351		HEATSINK ASS'Y			
2	1200-5-02		RIVET	CTC		
1	6200		HANDLE BLK.	STANFORD APPLIED		
2			LOCK NUT 2-56			
1	DB25S		CONNECTOR	CANNON	J201	
1	755381		TUNING UNIT BOARD ASS'Y			
1	TA-011157		METER BOARD ASS'Y			
1	BA-011960		+8V +12V BOARD ASS'Y			
1	BA-011471		-4V-8V-12V BOARD ASS'Y			
1	TA-011577		INTEGRATOR & BIT DETECTOR BD. ASS'Y			
1	TA-011756		DC RESTORER & LIMITER BD. ASS'Y			
1	TA-011540		DC RESTORER LIMITER PLUG IN BD. ASS'Y			
1	TA-011734		VCO BOARD ASS'Y			
1	TA-012105		PHASE COMPARATOR BOARD ASS'Y			
1	756584-1		MOTHER BOARD ASS'Y			
1	756184		FRONT PANEL			
-1	PART OR IDENTIFYING NO.	CODE IDENT	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

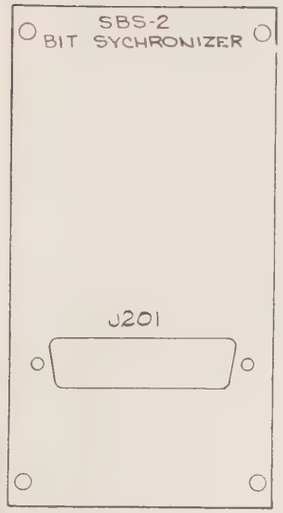
LIST OF MATERIALS

NOTES:

1. CONNECTOR No. 133-015-43; MATING CONNECTOR No. 143-015-01, AMPHENOL, SUPPLIED WITH UNIT
2. USE LOCTITE ON ALL SCREWS.
3. FOR WIRE LIST SEE DWG. No. 756212
4. ITEM 11 VARIES PER SPECIFIED BPS.
5. MATING CONNECTOR FOR ITEM 12 IS DB25P (CANNON) & JUNCTION SHELL P/N IS DB19678-2 (CANNON).

DRAWN	J. Anderson	10-30-67	DATA-CONTROL SYSTEMS, INC. DANBURY, CONN.
CHECKED	K.R. Buchanan	11-1-67	FINAL ASS'Y
PROJECT ENG	K.R.B.	11-1-67	BIT SYNCHRONIZER SBS-2
APPROVED			SIZE D — DWG. NO. 08539 — REV. 756282
MATERIAL			SCALE FULL — SHEET SBS-2
FINISH			
NEXT ASSY	USED ON		
APPLICATION			





SCREENED PANEL

2

NOTES:

1. STAMP P/N IN 1/8 HIGH CHARACTERS, APPROX. AS SHOWN, USING BLACK INDELIBLE INK, ON OPPOSITE SIDE.
2. SILKSCREEN PER DCS SPEC AS832004, COLOR TO BE BLACK USING NR 756275.

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM

LIST OF MATERIALS

756212	SBS-2
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED TOLERANCES ON:
.XXX ±.005 .XX ±.010
FRACTIONS ± 1/64 ANGLES ± 0°30'
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

CONTRACT NO.

		DATE
DRAWN	J. Anderson	8-14-67
CHECKED	[illegible]	8-25-67
DESIGNER	R. BURGESON	8-25-67
PROJECT ENG	[illegible]	8-25-67
APPROVED	[illegible]	8-15-67

MATERIAL 1/8 THK. 5052-H34 ALUM. ALY.

APPROVED

FINISH PER DCS SPEC AS 832008

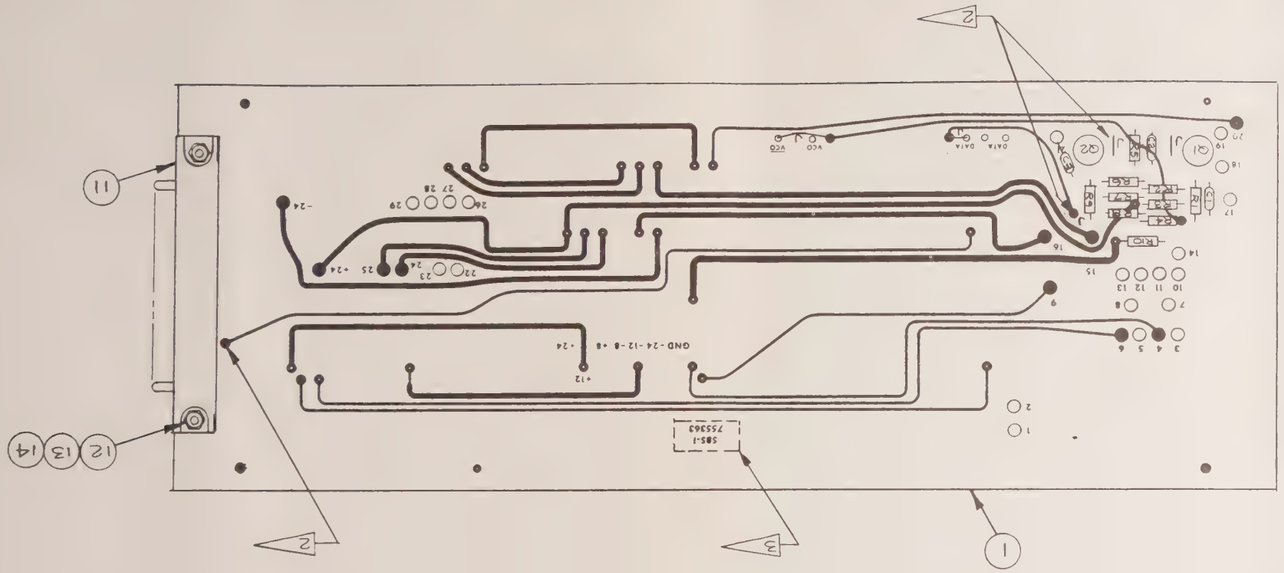
APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

FRONT PANEL
BIT SYCHRONIZER
SBS-2

SIZE	CODE IDENT.	
C	08539	756184

SCALE: FULL | SBS-2 | SHEET 1/1



NOTES:

1. ASSEMBLE PER DCS SPEC. QS-5000.
2. JUMPERS TO BE #22AWG SOLID WIRE.
3. REMOVE LETTERING INDICATED & STAMP PART NO. IN PLACE OF IT IN 1/8 HIGH CHARACTERS USING WHITE INDELIBLE INK.

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
	-1					
						15
2			NUT, LOCK #4-40	C.P.S.		14
2			WASHER, FLAT #4	C.P.S.		13
2			SCREW, P.H. SLOT. #4-40 x 5/8 LG.	C.P.S.		12
1	133-015-43		CONNECTOR	AMPHENOL		11
2	2N3642		TRANSISTOR		Q1 & Q2	10
1	MS35043-63		RESISTOR, 1/2W, 5% 100Ω		R10	9
1	MS35350-34		1/4W, 10Ω		R5	8
2	-100		5.6K		R4 & R8	7
2	-102		6.8K		R3 & R7	6
2	-82		1K		R2 & R6	5
2	MS35350-79		RESISTOR, 1/4W, 5%, 750Ω		R1 & R9	4
1	5C11		CAPACITOR, .47UF, 25V, ±20%	SPRAGUE	C2	3
2	DM10-221-F		CAPACITOR, 220PF; 500V ±1%	ARCO	C1, C3	2
1	755364		BOARD			1

LIST OF MATERIALS

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
XXX ± .XX ±
FRACTIONS ANGLES
FLATNESS WITHIN ⌒
HOLE TOLERANCE PER D C S SPECIFICATION AS-214018, CLASS 1
BREAK ALL CORNERS AND EDGES. REMOVE BURRS .015 MAX

CONTRACT NO.

DRAWN	R. J. Hobro	DATE 6/25/68
CHECKED	RW	6-25-68
DESIGNER	R. J. Hobro	6/25/68
PROJECT ENG.	B. Hammon	6/25/68
APPROVED		

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

BOARD ASSY
SBS-2

NEXT ASSY	USED ON
756282	SBS-2

APPLICATION

MATERIAL

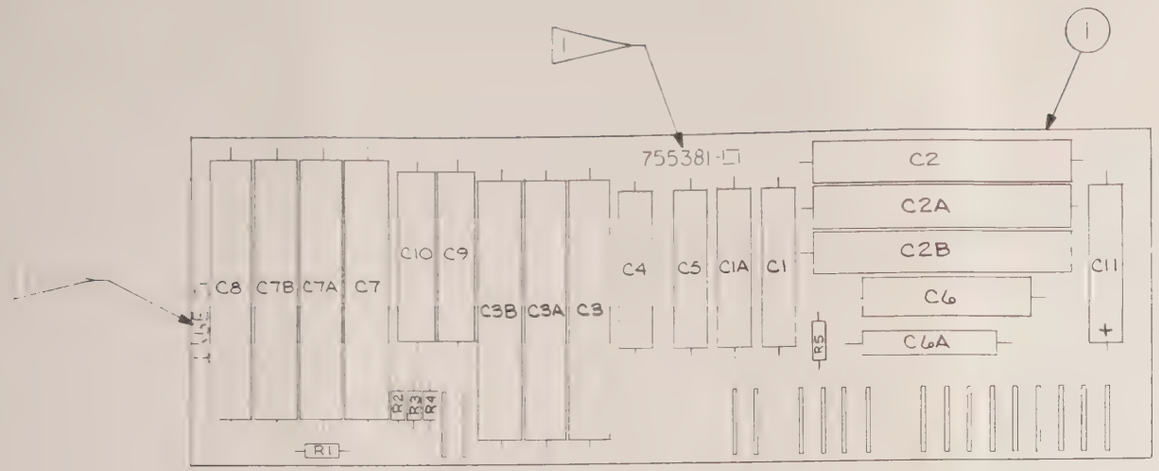
FINISH

APPROVED

APPROVED

SIZE	CODE IDENT	
C	08539	756584

SCALE FULL | SBS-2 | SHEET



PART No.	BIT RATE RANGE	TYPE No.
755381-1	10-16 BPS	1
-2	16-25	2
-3	25-40	3
-4	40-65	4
-5	65-100	5
-6	100-160	6
-7	160-250	7
-8	250-400	8
-9	400-650	9
-10	650-1000 BPS	10
-11	1-1.6 KBS	11
-12	1.6-2.5	12
-13	2.5-4	13
-14	4-6.5	14
-15	6.5-10	15
-16	10-16	16
-17	16-25	17
-18	25-40	18
-19	40-65	19
-20	65-100	20
-21	100-160	21
-22	160-250	22
-23	250-400	23
-24	400-650	24
-25	650-1000	25
755381-26	1000-1600 KBS	26

NOTES:

1. STAMP ASS'Y No., SIDE SHOWN, & TYPE No., ON OPPOSITE SIDE AS SHOWN, PER CHART IN 1/8 HIGH CHARACTERS, USING WHITE INDELIBLE INK.
2. FOR COMPONENT VALUES SEE LIST OF MATERIALS 756432.

QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT.	DESCRIPTION	SPECIFICATION OR VENDOR	SYMBOL	ITEM
			LIST OF MATERIALS			
A/R	2		CAPACITOR		C1-C11	3
A/R	2		RESISTOR		R1-R5	2
1	755339		BOARD SUB-ASS'Y			1

NEXT ASSY	USED ON
756282	SBS-2
755422	SBS-1
APPLICATION	

DIMENSIONS AND TOLERANCES PER MIL STANDARD 8
UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
.XXX ±.010 .XX ±.02
FRACTIONS ±1/64 ANGLES ±1°
FLATNESS WITHIN ⌒.
HOLE TOLERANCE PER D C S SPECIFICATION AS-814018, CLASS 1
BREAK ALL CORNERS AND EDGES, REMOVE BURRS .015 MAX

MATERIAL

FINISH

CONTRACT NO.

		DATE
DRAWN	F. Anderson	9-1-66
CHECKED	J.K. BURLINSON	9-6-66
DESIGNER	J.K. BURLINSON	9-6-66
PROJECT ENG	R. MENEGAY	10-7-66
APPROVED		

APPROVED

APPROVED

DATA-CONTROL SYSTEMS, INC.
DANBURY, CONN.

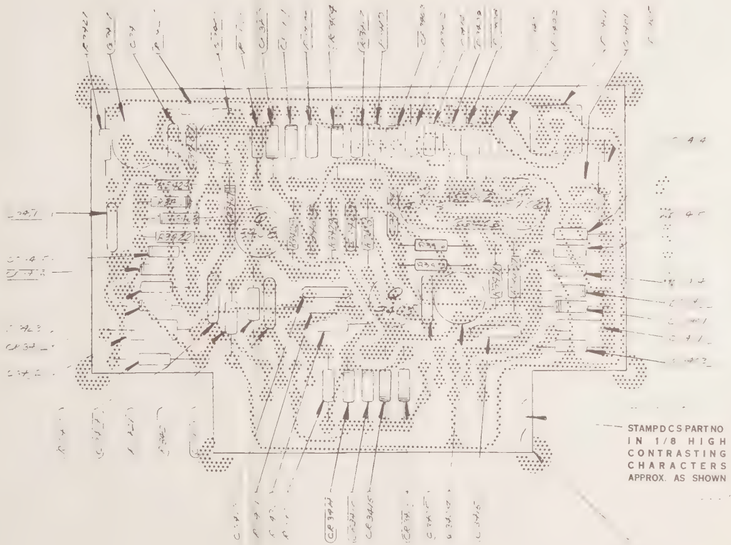
BOARD ASS'Y
TUNING UNIT
SBS/TU

SIZE	CODE IDENT.	
C	08539	755381

SCALE: FULL | SBS | SHEET

REV	DESCRIPTION	DATE	DWN	CHK	APP
B	CA 3[illegible]	[illegible]	[illegible]		
C	[illegible]	[illegible]	[illegible]		
D	CA-3849-CHG'D QTY. E	7/1/6	[illegible]		
E	CA-4479 CHG'D DIODE VALUES	8/21/68	[illegible]	[illegible]	[illegible]

ADD TRANSPARENT SLEEVING TO COMPONENTS HAVING COPPER UNDERNEATH ON COMPONENT SIDE



STAMP D C S PART NO IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

REF	DESCRIPTION	QTY

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY / ASSY
			BOARD, PAB METER	1
			POT 1 K Ω 201-10 WA	1
			RES. RN CR VALUE 10% 1/4 W	1
			22K	1
			RES ELECTRO FILM 1/4W, 10% 10 K	1
			[illegible]	1
			[illegible]	1
			[illegible]

REV	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-3190-CHG'D COMPONENTS	3/1/66	P.I		
C	CA-3190-2 CHG'D R3401, R3403 P/N	3/16/66	P.I		
D	CA-4479 CHGD DIODE VALUE	8/26/68	[illegible]		

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY

TW-012514 REV D

SKETCH SHOWING LOCATION OF TEST POINT

NOTES:
1. △ ELCO PIN CONNECTIONS TO CU. MOTHER BD 3G00
2. REF. ASSY TA-011137
3. REF. BLOCK DIAGRAM, DB-01331E
4. ALL RESISTORS ARE AB, CB, 1/4W, 10% UNLESS OTHERWISE NOTED.

REF	DESCRIPTION	QTY

GPS-3 FIRST PRODUCT — NEXT ASSEMBLY

DATA CONTROL SYSTEMS, INC.

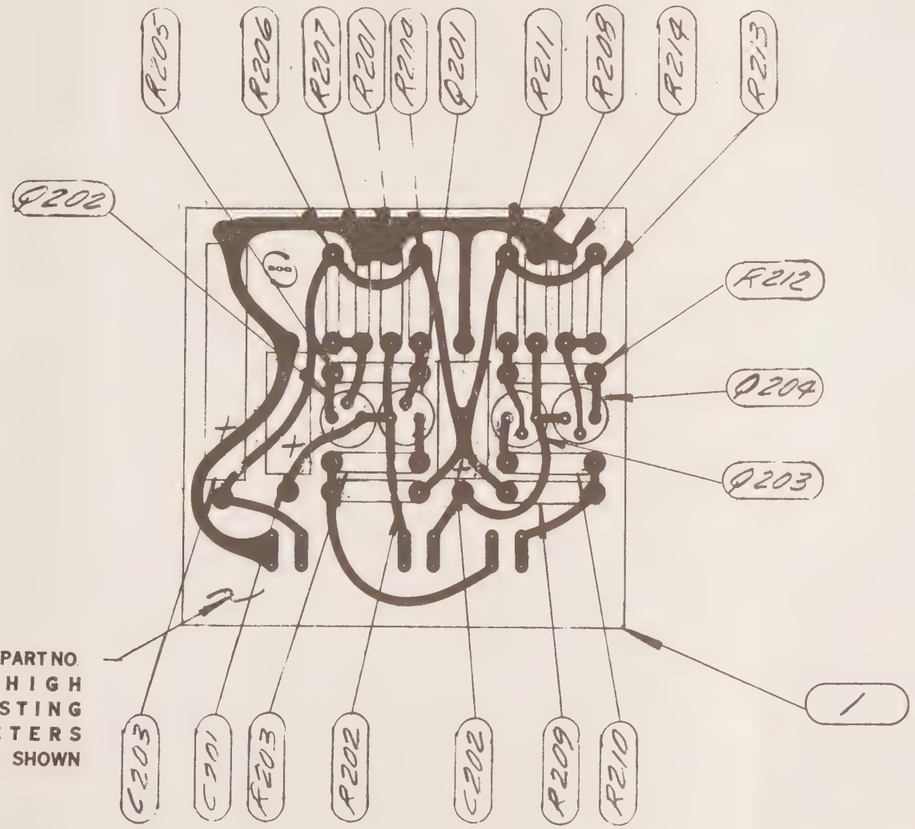
TITLE: SCHEMATIC, METER BD CONTROL UNIT

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .002
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0° 30'
FLATNESS WITHIN ⏥ / IN
FRACTIONAL HOLES Ø ± .004
NOTE: BREAK ALL SHARP CORNERS .005" - .015"
SURFACE FINISHES NOT TO EXCEED

	DATE
DWN. DH	1/24/68
CHKD. [illegible]	1/24/68
ENG. [illegible]	1/24/68
APP. [illegible]	1/24/68
SCALE	

DO NOT SCALE DRAWING
MAT'L
FINISH
TW-012514 REV D
SHEET

REV	DESCRIPTION	DATE	DWN	CHK	APP
B	SERIES WAS 300 R&E	3/27/64	PJH	RWG	RKZ
C	ADDED STAMP P/N NOTE R&E	7/14/64	PJH	WF	WF
D	CA-3190 CHG'D. COMPONENTS	3/18/66	P.I.		
E	CA-3929 - CHG'D. RES. VALUES	9/19/66	PI		
F	CA-3749 CHG'D COMP. VALUES	5/29/67	JCP		
G	CA-3749-1 CHG Q201 & Q203	1/15/68	JCP	JR	JR
H	CA-4354 CHG'D Q201 & Q203	3/29/68	JP	JR	JR



STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN

BA-011460 REV H

ITEM	SYMBOL	DWG NO	DESCRIPTION	QTY/ASSY
1		BF-010660	BOARD FAB	1
*	R 201		RES. AB,EB, 1/4W, 10% 4.7K	1
*	R 202		82Ω	1
*	R 203		120Ω	1
*	R 204		1K	1
*	R 205		1.8K	1
*	R 208		1.8K	1
*	R 209		82Ω	1
*	R 210		150Ω	1
*	R 211		1K	1
*	R 212		2.2K	1
	R 206		RES. T.I, CC 1/4, 1/4W, 1% 909Ω	1
	R 207		1.0K	1
	R 213		909Ω	1
	R 214		511Ω	1
	Q 201	NO SECOND CHO:	TRANS. MOTOROLA 2N3206	1
	Q 202		TRANS. G.E, 2N3391A	1
	Q 203	NO SECOND CHOICE	TRANS. MOTOROLA 2N3904	1
	Q 204		TRANS. G.E, 2N3391A	1
	C 201		CAP. SPRAGUE TE 1160 15V, 50MF	1
	C 202		CAP, 15V, 50MF	1
	C 203		CAP, SPRAGUE TE 1307 50V, 50MF	1

NOTE

1. * PER MS35043

REF	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY/ASSY
GPS-5	DA-011852	1

DATA CONTROL SYSTEMS, INC.

TITLE BOARD ASSY- +8V, +12V POWER SUPPLY

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0° 30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES .0 + 1/64
NOTE- BREAK ALL SHARP CORNERS .005" - .015"
SURFACE ROUGHNESS NOT TO EXCEED ~

	DWN	DATE
	PJH	9/19/63
CHKD	RKZ	9/24/63
ENG	GM/WF	10/14/63
APP.	WF	10/14/63
SCALE	FULL	

DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

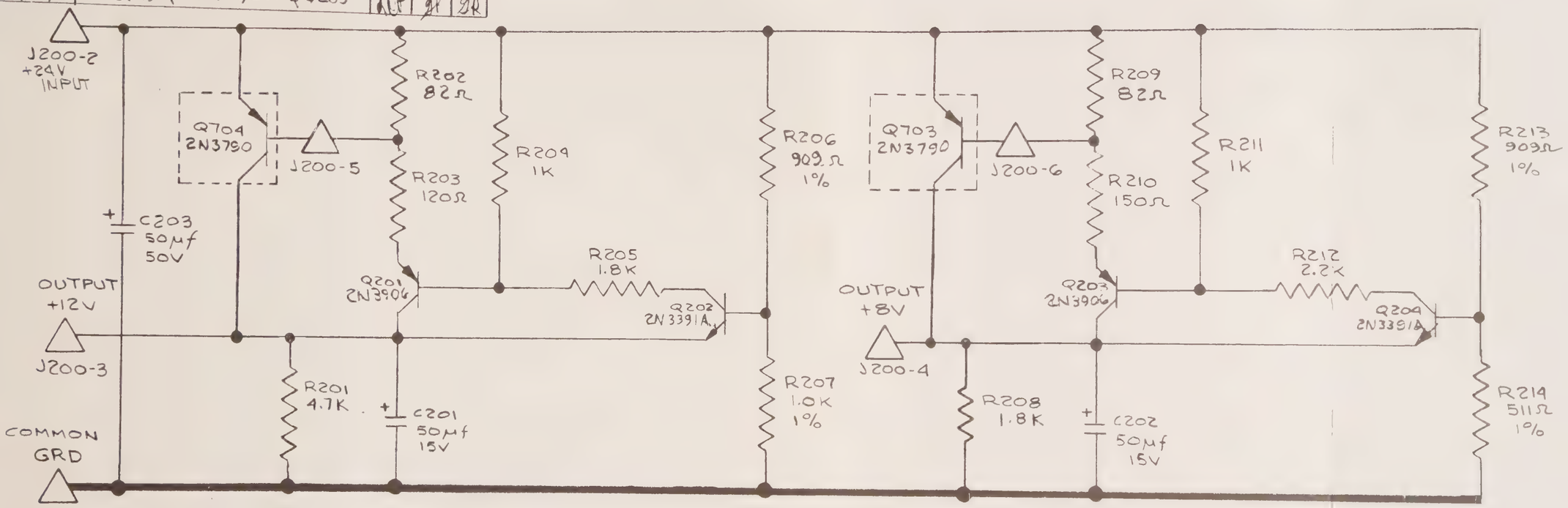
BA-011460 REV H

SHEET

REV.	DATE	DESCRIPTION	BY	CHK'D	ENG APP'D
B	3/3/65	CA-2824-C203 WAS C303			
C	3/8/66	CA-3190-CHG'D. COMPONENTS	P.I		
D	9/9/66	CA-3190-2 CHG'D. Q704, 703 TO 2N3790	P.I		
E	9/13/66	CA-3429-CHGD. RES. VALUES	PI		
F	5/29/67	CA-3749 CHG'D. COMP. VALUES			
G	1/19/68	CA-3749-1 CHG Q201 & Q203			

H | CA-4354 CHG. TRANS. TYPE | 1/29 | BW-012745 | H

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY



NOTES:

1. △ ELCO PIN CONNECTIONS TO PWP SUP MOTHER BD 600
2. Q703 & Q704 ARE PART OF ASSY CA-011449
3. REF. ASSY BA-011460
4. REF. BLOCK DIAGRAM DB-013312
5. RESISTORS ARE AB, EB, 1/2W, 10% UNLESS OTHERWISE NOTED

REF.	DESCRIPTION	QTY

GPS-5	~	~
PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, +8V+12V POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0, + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"

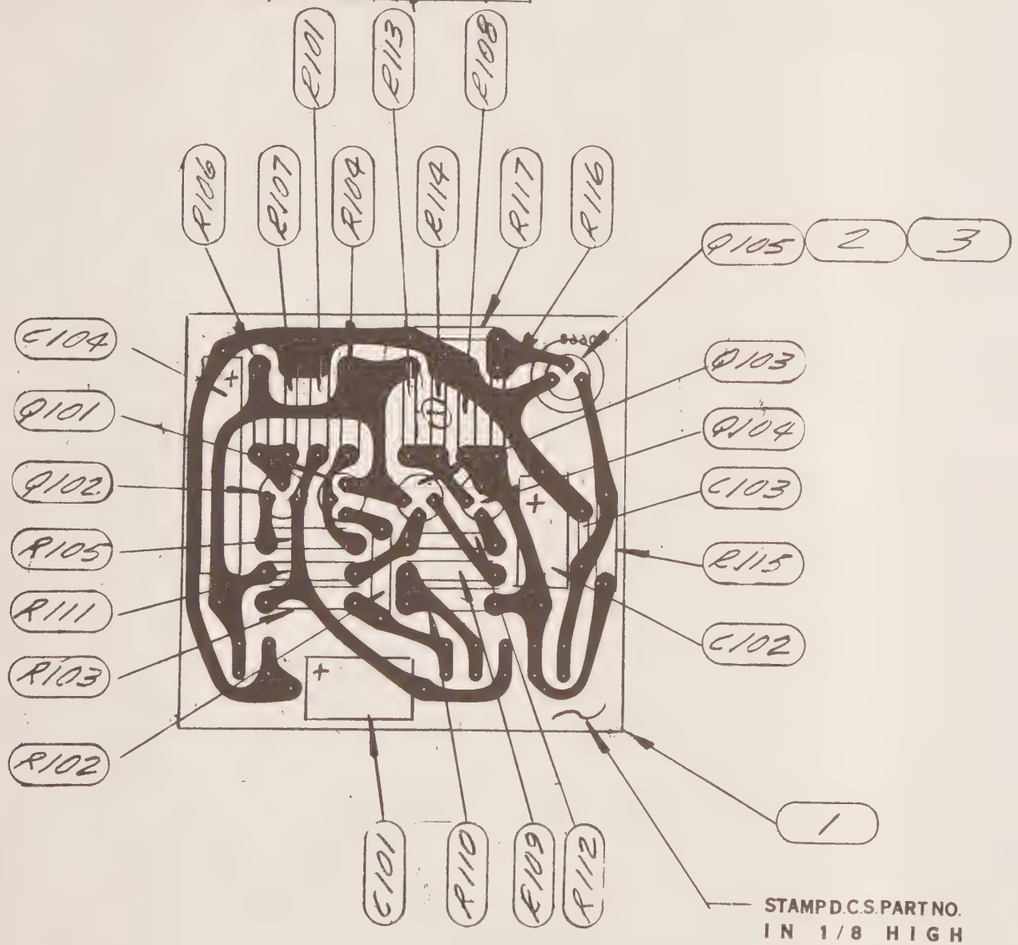
		DATE
DWN.	DH	9/23/64
CHK'D.		1/19/65
PROJ. ENG.		1/26/65
CH. ENG.		2/16/65
SCALE	~	

DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

BW-012745 REV. H

REV.	DESCRIPTION	DATE	DWN	CHK.	APP.
C	SERIES WAS 200 REF	3/25/64	PJH	RWG	
D	ADDED STAMP P/N NOTE REF	7/14/64	PJH		
E	CR-2554-R106 WAS 935Ω	7/31/64		RWG	
F	CA-3190-CHG'D COMPONENTS	3/16/66	PI		
G	CA-3429-CHG'D RES. VALUES	9/16/66	PI		
H	CA-3749 CHG COMP. VALUES			5/29/68	
J	CA-4354 CHG'D TRANS			3/29/63	

BA-011871 REV J



NOTE:

1. * PER MS 35043

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
1		BA-010668	BOARD FAB.	1
2			PAD MILTON ROSS A-10068	1
3			HEAT SINK-DNF207 WAKEFIELD ENG. INC.	1
*	R101		RES. AB EB 1/4W 1% 4.7K	1
*	R102		120Ω	1
*	R103		82Ω	1
*	R104		1K	1
*	R105		1.8K	1
*	R108		1.3K	1
*	R109		150Ω	1
*	R110		82Ω	1
*	R111		1K	1
*	R112		2.2K	1
*	R115		1K	1
	R106		RES. T.I., CG 1/4, 1/4W, 1% 909Ω	1
	R107		1.00K	1
	R113		909Ω	1
	R114		511Ω	1
	R116		511Ω	1
	R117		464Ω	1
	C101		CAP. SPRAGUE TE1160, 15V, 50MF	1
	C102		CAP. 15V, 50MF	1
	C103		CAP. SPRAGUE 20% 5C11, 25V 0.47MF	1
	C104		CAP. SPRAGUE TE1307, 50V, 50MF	1
	Q101		TRANS. GE, 2N3391A	1
	Q102	NO SECOND CHOICE	TRANS. MOTOROLA 2N3906	1
	Q103		TRANS. GE, 2N3391A.	1
	Q104	NO SECOND CHOICE	TRANS MOTOROLA 2N3906	1
	Q105		TRANS. SPRAGUE, TN538	1

REF.	DESCRIPTION	QTY

PRODUCT	NEXT ASSEMBLY	QTY./ASSY.
GPS-5	BA-011452	1

DATA CONTROL SYSTEMS, INC.

TITLE: BD. 455Y- -9V, -8V, -12V POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES .0. ± 1/64
NOTE- BREAK ALL SHARP CORNERS .005" - .015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN	PJH	9/15/63
CHKD		10/15/63
ENG.		10/15/63
APP.		10/15/63
SCALE	FULL	

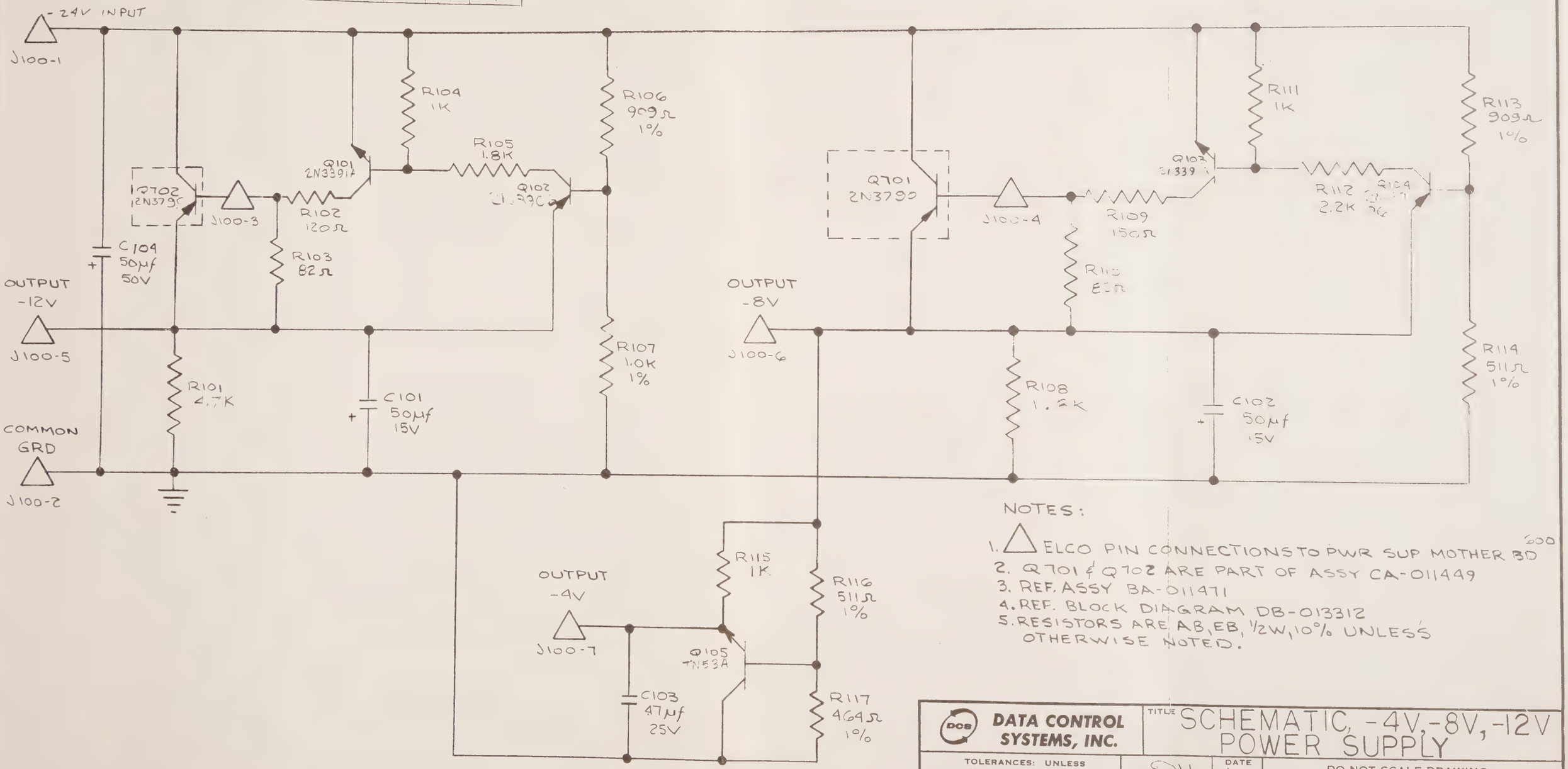
DO NOT SCALE DRAWING
MAT'L
FINISH

BA-011871 REV J

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2824-SYMBOL C104 WAS C204	9/4/65	RW	RWG	W.
C	CA-3190-CHG'D. COMPONENTS	3/18/66	P. I.		
D	CA-3190-2 CHG'D. Q701, Q702 TO 2N3790	9/12/66	P. I		
E	CA-3429-CHG'D. RES. VALUES	9/10/66	P I		
F	CA-3749 CHG'D COMP VALUES	9/23/69	DH	SPM	
G	CA-4354 CHG'D TRANS TYPE	3/29/72	DF	JR	DR

BW-012744 REV. G

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY.



NOTES:

1. △ ELCO PIN CONNECTIONS TO PWR SUP MOTHER BD 600
2. Q701 & Q702 ARE PART OF ASSY CA-011449
3. REF. ASSY BA-011471
4. REF. BLOCK DIAGRAM DB-013312
5. RESISTORS ARE AB, EB, 1/2W, 10% UNLESS OTHERWISE NOTED.

REF.	DESCRIPTION	QTY

GPS-5		
PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, -4V, -8V, -12V POWER SUPPLY

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED

	DWN.	DATE
	DH	9/23/69
CHKD.		
ENG.		
APP.		
SCALE		

DO NOT SCALE DRAWING
MAT'L
FINISH

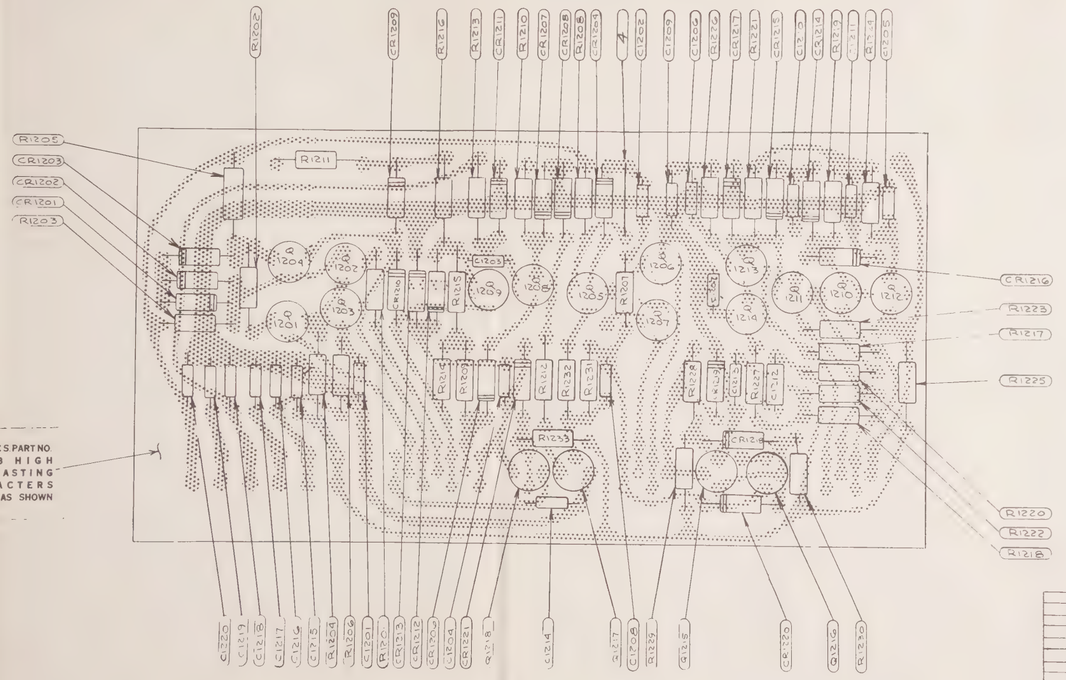
BW-012744 REV. G

SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2878-Q1205 WAS 2N935A	4/16/66	[illegible]		
C	CA-3190-CHGD COMPONENTS	3/31/66	P. [illegible]		
D	CA-5191-CHG'D C-1 TO C-2	5/2	[illegible]		
E	CA-3190-2-CHGD SCHEM FROM 2N3694 TO 2N3691	9/12/66	DT		
F	CA-3849-CHG'D CAP. STYLE	7/11/67	DT		
G	CA-4456 CHG CAP VOLTAGE	8-29-68	RV	BR	BR
H	CA-4479 CHG'D DIODE VALUES	2-7-69	JL	BR	BR

NOTES:
1. INSTALL ITEM 2 UNDER Q1201, Q1204, Q1205 Q1206, & Q1207.
2. INSTALL ITEM 3 UNDER Q1202, Q1203, Q1212, Q1213, Q1208, Q1209, Q1210, Q1211 Q1214, Q1215, Q1216, Q1217, & Q1218
3. ALL ALLEN BRADLEY CB, 1/4W, 10% RESISTORS TO CONFORM TO MS35350.

STAMP DCS PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN



REF	DESCRIPTION	QTY

TA-011577 REV. H

	DIODE, SOLITRON	CER 69	1
	FAIRCHILD	1N3600	1
		1N3600	1
	SOLITRON	CER 69	1
		1N3067	1
		1N3067	1
	CONT. DEVICE,	1N3067	1
		1N3067	1
		1N3067	1
		1N3067	1
		1N3067	1
		1N3067	1
	DIODE	1N3067	1
		1N3067	1
	TRANS, FAIRCHILD	2N3638	1
Q1204		2N3638	1
Q1205		2N3640	1
Q1206		2N3640	1
Q1207		2N3640	1
Q1202	TRANS, G.E.	2N3391A	1
Q1203		2N3391A	1
Q1212		2N3856A	1
Q1213		2N3856A	1
Q1208	TRANS, G.E.	2N3682	1
Q1209	TRANS, FAIRCHILD	2N3640	1
Q1210	TRANS, T.I.,	2N706A	1
Q1211		2N706A	1
Q1214	TRANS, MOTOROLA	2N3906	1
Q1215	TRANS, FAIRCHILD	2N3640	1
Q1216		2N3640	1
Q1217		2N3640	1
Q1218		2N3640	1
C1201	CAP, SPRAGUE, 3C15	.047μf	1
C1205		.047μf	1
C1206		.047μf	1
C1207		.047μf	1
C1202	CAP, ERIE	831-050-Z5F0-151K, 150μμf	1
C1203		831-000-U2J0-220K, 22μμf	1
C1204		831-000-U2J0-330K, 33μμf	1
C1208		330K 33μμf	1
C1209	CAP, SPRAGUE, 5C13	.10μf	1
C1210		.10μf	1
C1211		1.0μf	1
C1212	CAP, SPRAGUE, 5C13	1.0μf	1
C1213		1.0μf	1
C1214		1.0μf	1
C1215		1.0μf	1
C1216		1.0μf	1
C1217		1.0μf	1
C1218		1.0μf	1
C1219		1.0μf	1
C1220		1.0μf	1

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY
1		CF-01072G	BD FAB	1
2			PAD, TRANS, R055 A10042	5
3			A10042	13
	R1201		RES., AB, CB, 1/4W, 10%, 330Ω	1
	R1203		12K	1
	R1206		150Ω	1
	R1207		100Ω	1
	R1208		82K	1
	R1209		1.8K	1
	R1210		3.9K	1
	R1214		1.0K	1
	R1217		1.2K	1
	R1218		150Ω	1
	R1219		2.7K	1
	R1220		1.5K	1
	R1221		2.7K	1
	R1222		150Ω	1
	R1223		1.2K	1
	R1224		100Ω	1
	R1226		160Ω	1
	R1227		100Ω	1
	R1228		100Ω	1
	R1229		EB, FW107, 8K	1
	R1230		CB, FW107, 8.9K	1
	R1231		1.2K	1
	R1232		5.6K	1
	R1233		3.7K	1
	R1212		RES., AB, EB, 1/2W, 10% 270Ω	1
	R1213		270Ω	
	R1225		2.[illegible]	
	R1202		RES. ELECTRA MF56-D 1/4W, 1% 2.49K	
	R1204		2.81K	
	R1205		3.01K	
	R1211		1.23K	
	R1215		2.61K	
	R1216		2.00K	
	CR1201		DIODE, CONT DEVICES, 1N3067	1
	CR1202		1N3067	1
	CR1203		DIODE, 1N3067	1
	CR1204		CONT. DEVICE 1N3067	1
+			SEE BACK SIDE	1
	CR1206		DIODE CONT. DEV. 1N3067	1
	CR1207		1N3067	1

GPS-5 FIRST PRODUCT | CA-012472 NEXT ASSEMBLY | 1 QTY/ASSY

DATA CONTROL SYSTEMS, INC.

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN /IN.
FRACTIONAL HOLES -0 + 1/64
NOTE: BREAK ALL SHARP CORNERS .005", .015" SURFACE ROUGHNESS NOT TO EXCEED ✓

TITLE: BD ASSY, INTEGRATOR & BI DETECTOR
DO NOT SCALE DRAWING

		DATE
DWN.	[illegible]	3/19/64
CHKD.	HS	9/11/64
ENG.	[illegible]	11/16/64
APP.	[illegible]	11/17/64
SCALE		

MAT'L
FINISH

TA-011577 REV.

SHEET

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2838 - J1200-19 WAS J1200-9	11/3/65	[illegible]	[illegible]	HM
C	CA-2878 - Q1208 WAS 2N955A	2/3/66	[illegible]	[illegible]	[illegible]
D	CA-3190 - CHG'D. COMPONENTS	3/10/66	R. I.	[illegible]	[illegible]
E	CA-3191-1 - CHG'D. VALUE OF CAB. (9FE) OMITTED CR1205	3/23/66	R. I.	[illegible]	[illegible]
F	CA-3190-2 CHG'D. CR1209 FROM 2N3600 TO 1N3600	9/16/66	R. I.	[illegible]	[illegible]
G	CA-4456 CHGD CAP VOLTAGE	9-29-68	R.	MR	MR
H	CA-4381 REVISED SCHE.	8-6-68	R.	MR	MR
J	CA-4479 CHG DIODES	8-12-69	MR	MR	MR
K	CA-4697 REVISED DWG.	9-5-68	MR	MR	MR

REF.	DESCRIPTION	QTY

TW-012721 REV. K

ITEM	SYMBOL	DWG. NO	DESCRIPTION	QTY. /ASSY.

NOTES
1) △ELCO PIN CONN TO MOTHER BOARD
2) REF ASSY TA-011577
3) RES. ARE ¼W, CB, ¼W, 10% UNLESS OTHERWISE NOTED
4) REF BLOCK DIAGRAM DB-013312

+24V J1200-1
+12V J1200-2
+8V J1200-3
FROM FCB J1200-9
FROM LIMITER J1200-11
FROM VCO J1200-18
VCO J1200-15
VCO J1200-14
GRD J1200-7
-4V J1200-8
-8V J1200-4
-12V J1200-5
-24V J1200-6
DATA J1200-19
DATA TP1201
DATA J1200-22
DET TEST JACK ON FRONT PANEL
INTEGRATING DET CAP IN TU
MONOSTABLE CAP IN TU
DATA INVERTING SW ON CU FRONT PANEL

C1220 1.0μf
C1219 1.0μf
C1218 1.0μf
C1214 1.0μf
C1217 1.0μf
C1216 1.0μf
C1215 1.0μf
C1213 1.0μf
C1212 1.0μf
C1210 1.0μf
C1211 1.0μf
C1209 1.0μf
C1208 33μμf
C1207 .047μf 25V.
C1206 .047μf 25V.
C1205 .047μf 25V.
C1204 33μμf
C1203 22μμf
C1202 150μμf
C1201 .047μf 25V.

R1201 330Ω
R1202 6.19K 1%
R1203 12K
R1204 2.81K 1%
R1205 3.01K 1%
R1206 150Ω
R1207 100Ω
R1208 8.2K
R1209 1.8K
R1210 3.9K
R1211 1.33K 1%
R1212 270Ω ½W
R1213 270Ω ½W
R1214 1K
R1215 2.61K 1%
R1216 2.0K 1%
R1217 1.2K
R1218 150Ω
R1219 2.7K
R1220 1.5K
R1221 2.7K
R1222 150Ω
R1223 1.2K
R1224 100Ω
R1225 2.7K ½W
R1226 100Ω
R1227 100Ω
R1228 100Ω
R1229 1.8K ½W, 10%
R1230 3.3K
R1231 1.2K
R1232 5.6K
R1233 2.7K

CR1201 IN3067
CR1202 IN3067
CR1203 IN3067
CR1204 IN3067
CR1205 IN3067
CR1206 IN3067
CR1207 IN3067
CR1208 CER69
CR1209 IN3600
CR1210 IN3600
CR1211 CER69
CR1212 IN3067
CR1213 IN3067
CR1214 IN3067
CR1215 IN3067
CR1216 IN3067
CR1217 IN3067
CR1218 IN3067
CR1219 IN3067
CR1220 IN3067
CR1221 IN3067

Q1201 2N3638
Q1202 2N3391A
Q1203 2N3391A
Q1204 2N3638A
Q1205 2N3638A
Q1206 2N3638A
Q1207 2N3638A
Q1208 2N3692
Q1209 2N3694
Q1210 2N706A
Q1211 2N706A
Q1212 2N3638A
Q1213 2N3638A
Q1214 2N3640
Q1215 2N3640
Q1216 2N3640
Q1217 2N3640
Q1218 2N3640
Q1219 2N3638A

GPS-9

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, INTEGRATOR & BIT DETECTOR

DO NOT SCALE DRAWING

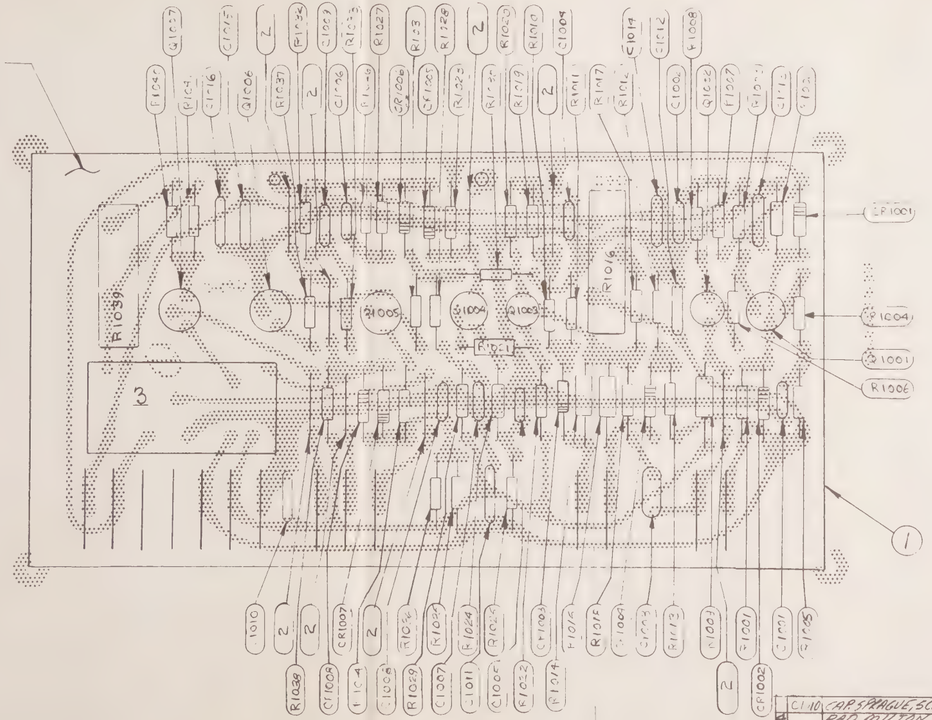
TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~/IN.
FRACTIONAL HOLES .0 + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT

	DWN	DATE
DWN	[illegible]	1/22/65
CHKD	[illegible]	1/23/65
ENG.	[illegible]	[illegible]
APP.	[illegible]	[illegible]
SCALE		
MAT'L		
FINISH		

TW-012721 REV. K

REV	DESCRIPTION	DATE	DWN	CHK	APP
B	A-3 P.C. [illegible]	[illegible]	[illegible]	[illegible]	[illegible]
C	CA-3849 CHG'D CAP, STYLE	7/10/67	[illegible]		

STAMP D.C.S. PART NO. IN 1/8 HIGH CONTRASTING CHARACTERS APPROX. AS SHOWN



NOTE
1. INSTALL ITEM 4 UNDER Q1005, 1006, & 1007
2. INSTALL ITEM 5 UNDER Q1001, Q1002, Q1003, & 1007
3. ALL ALLEN BRADLEY CB, 1/4W 10% RESISTORS TO CONFORM TO MS 35220.

TA-011756

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY. PER ASSY
	R1035		RES. CB, 1/4W, 10% 47Ω	1
	R1036		2.7K	1
	R1037		330Ω	1
	R1038		2.7K	1
	R1039		2.2K	1
	R1040		15K	1
	R1041		RES. AB, EB, 1/2W, 10% 2.2K	1
	R1042		RES. ELECTRA MFG'S O: 1/4W, 1% 14.7K	1
	R1043		RES. 14.7K	1
	R1044		POT. BOURNS "3067P 10% 10K	1
	R1045		POT. BOURNS "3067P 202 2K	1
	CR1001		DIODE, CONT. DEVICE, IN306	1
	CR1002		DIODE, IN3067	1
	CR1003		DIODE, CONT. DEVICES IN3067	1
	CR1004		DIODE, IN3067	1
	CR1005		DIODE, IN3067	1
	CR1006		DIODE, IN3067	1
	CR1007		DIODE, IN3067	1
	CR1008		DIODE, IN3067	1
	Q1001		TRANS. MOTOROLA, 2N3905	1
	Q1002		TRANS., G.E., 2N3391A	1
	Q1003		TRANS., 2N3391A	1
	Q1004		TRANS., MOTOROLA, 2N3906	1
	Q1005		TRANS., 2N3393	1
	Q1006		TRANS., 2N3393	1
	Q1007		TRANS., 2N3393	1
	C1001		CAP, SPRAGUE, "5C15, 25V, 20% .047MF	1
	C1002		CAP, .047MF	1
	C1003		CAP, ERIE 831-000-X5R[illegible]51K, 150MF	1
	C1004		CAP, SPRAGUE, "5C15, 25V, 20% .047MF	1
	C1005		CAP, .047MF	1
	C1006		CAP, .047MF	1
	C1007		CAP, .047MF	1
	C1008		CAP, .047MF	1
	C1009		CAP, .047MF	1
	C1010		CAP, SPRAGUE, 5C13, 25V, 20% 1.0MF	1
	C1011		CAP, SPRAGUE, 5C13, 25V, 20% 1.0MF	1
	C1012		CAP, 1.0MF	1
	C1013		CAP, 1.0MF	1
	C1014		CAP, 1.0MF	1
	C1015		CAP, 1.0MF	1
	C1016		CAP, 1.0MF	1
	C1017		CAP, 1.0MF	1

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY. PER ASSY
1		BF-011290-	BOARD, FAB	1
2			JUMPER #22 BUS WIRE	5
3		TA-011540-	PLUG-IN BOARD ASSY	1
	R1001		RES. AB, CB, 1/4W, 10% 1.0K	1
	R1002		12K	1
	R1003		12K	1
	R1004		150Ω	1
	R1005		150Ω	1
	R1006		150Ω	1
	R1007		56Ω	1
	R1008		56Ω	1
	R1010		5.6K	1
	R1011		270Ω	1
	R1012		270Ω	1
	R1013		5.6K	1
	R1017		470K	1
	R1018		220Ω	1
	R1019		50	1
	R1020		150	1
	R1021		150	1
	R1022		57K	1
	R1023		5.6K	1
	R1024		56	1
	R1025		56	1
	R1026		300Ω	1
	R1027		2.7K	1
	R1028		1K	1
	R1029		330Ω	1
	R1030		680Ω	1
	R1031		150Ω	1
	R1032		150Ω	1
	R1033		1.2K	1
	R1034		330Ω	1

REF	DESCRIPTION	QTY

GPS-5 | CA-012472 | 1

FIRST PRODUCT | NEXT ASSEMBLY | QTY. / ASSY

DATA CONTROL SYSTEMS, INC.

TITLE: BOARD ASSY DC RESTORER & LIMITER

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN .../IN.
FRACTIONAL HOLES Ø ± 1/64
NOTE BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ✓

	DWN	CHKD	ENGR	APP
DATE	7/26/67	7/27/67	11/1/67	11/9/67

DO NOT SCALE DRAWING

MAT'L
FINISH
SCALE 2-1

TA-011756 REV C

SHEET

REV	DESCRIPTION	DATE	DWN	CHK	APP
C	CA-2787-PRSTD FITTED MODULE LAYOUT				
D	CA-3193-CHG'D. COMPONENTS				

TW-012723 REV D

ITEM	SYMBOL	DWG NO	DESCRIPTION	QTY PER ASSY

MONITOR JACK FRONT PANEL OF CONTROL UNIT

+24V J1000-1

+12V J1000-2

DATA INPUT TO SYNCHRONIZER J801

DATA INPUT J1000-14

DATA SYMMETRY R1039

LIMITER CENTERING R1016

TP1002 TP1001

SKETCH SHOWING LOCATION OF TEST POINTS

GRD J1000-7

-12 J1000-5

-24 J1000-6

TP1001 DC RESTORER

TP 002 LIMITER

R1001 1K
R1002 12K
R1003 12K
R1004 150Ω
R1005 150Ω
R1006 150Ω
R1007 56Ω
R1008 56Ω
R1009 2.2K ½W
R1010 5.6K
R1011 270Ω
R1012 270Ω
R1013 5.6K
R1014 14.7K 1%
R1015 14.7K 1%
R1016 10K
R1017 470K
R1018 220Ω
R1019 150Ω
R1020 150Ω
R1021 150Ω
R1022 39K
R1023 5.6K
R1024 56Ω
R1025 56Ω
R1026 820Ω
R1027 6.8K
R1028 12K
R1029 3.3K
R1030 680Ω
R1031 150Ω
R1032 180Ω
R1033 2.2K
R1034 330Ω
R1035 47Ω
R1036 2.7K
R1037 330Ω
R1038 2.7K
R1039 2K
R1040 2K

C1001 .047μf
C1002 .047μf
C1003 150μμf
C1004 .047μf
C1005 .047μf
C1006 .047μf
C1007 .047μf
C1008 .047μf
C1009 .047μf
C1010 1.0μf
C1011 1.0μf
C1012 1μf
C1013 1.0μf
C1014 1.0μf
C1015 1.0μf
C1016 1.0μf

CR1001 IN3067
CR1002 IN3067
CR1003 IN3067
CR1004 IN3067
CR1005 IN3067
CR1006 IN3067
CR1007 IN3067
CR1008 IN3067

Q1001 2N3906
Q1002 2N3391A
Q1003 2N3391A
Q1004 2N3906
Q1005 2N3906
Q1006 2N3906
Q1007 2N3906

J1000-11
J1000-19
J1000-12

DC RESTORER CAPS IN TU

LIMITER CENTERING

DATA SYMMETRY

TA-011540 ASSY

A B C D E F G H J

J1000-C TO PHASE COMPARATOR BD 1700 THRU DOUBLER CAP IN TU

FROM FCB DCAMP ON BD 1100 J1000-8

J1000-9 TO INTEGRATING BIT DETECTOR BD 1200

NOTES:
1. △ ELCO PIN CONNECTIONS TO MOTHER BD 1500
2. REF. ASSY TA-011756
3. REF. BLOCK DIAGRAM DB-013312
4. RESISTORS AB, CB, ⅛W, 10% UNLESS OTHERWISE NOTED

REF	DESCRIPTION	QTY

GPS-S FIRST PRODUCT | NEXT ASSEMBLY | REF. QTY —EACH

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, DC RESTORER & LIMITER

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES Ø .+ 1/64
NOTE: BREAK ALL SHARP CORNERS .008"-.018"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN	DH	9/17/64
CHKD	[illegible]	11/18/65
ENG	[illegible]	11/4/66
APP	[illegible]	11/4/66
SCALE	~	

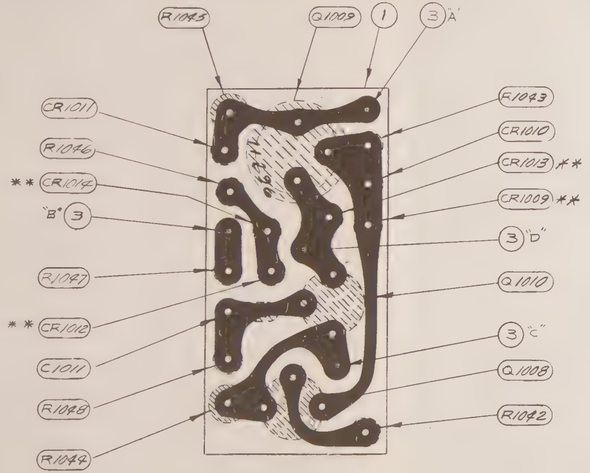
DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

TW-012723 REV D

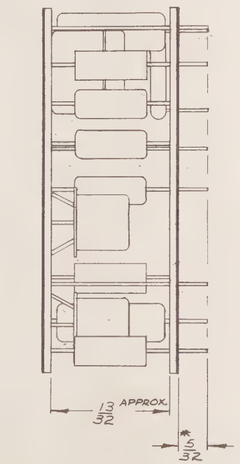
SHEET

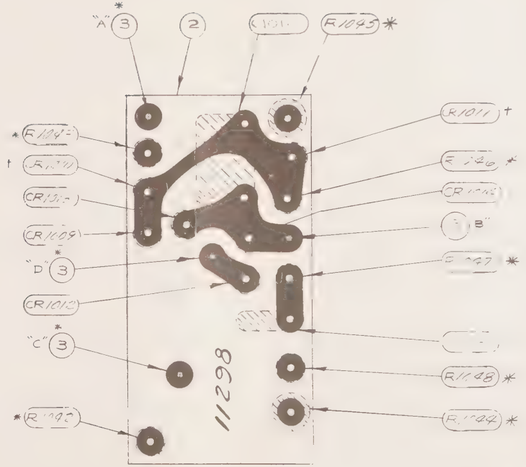
B	SERIES CALLOUT WAS 500, R592 WAS 1.93K, R593 WAS 1.62K. (B&C)	10/10/63	DJH	WY	WY
C	SERIES CALLOUT WAS 100 28E	3/13/64	DJH	KWG	

D	CA-3180-CH3 COMPONENTS		
E			
F	CA 4413 CHG'D Q1008 & Q1010	4-17-64	
G	CA 4410 CHG'D CAP. CALLOUTS	6-1-64	



VIEW "B"





NOTES:
- △ PER MS 35350
- * LEADS TO EXTEND 5/32 FROM COPPER SIDE OF ITEM 2.
- ** DIODE TO BE MOUNTED WITH CATHODE UP. A,B,C & D OF ITEM 1 TO CORRESPOND TO A,B,C & D OF ITEM 2. (SEE VIEW "B")
- + DIODE TO BE MOUNTED WITH CATHODE DOWN (SEE VIEW "B")

CATHODE

		BF-011296	UPPER PLUGIN BD. FAB
	2	BF-011298	LOWER PLUG-IN BD. FAB
	3		JUMPER #22 BUSS WIRE A/R
△	R1042		RES. AB,CB, 1/4W, 10% 50Ω
△	R1043		RES., 10K
	R1044		RES., T.I. CG 1/4, 1/4W, 1% 1.1K
	R1045		RES., T.I. CG 1/4, 1/4W, 1% 6.19K
△	R1046		RES., AB,CB, 1/4W, 10% 2K
△	R1047		RES. 10Ω
△	R1048		RES. 150Ω
	Q1008		TRANS.,
	Q1009		TRANS. SPRAGUE,
	Q1010		TRANS.
			CAP. SPRAGUE, TYPE 3CI5, 25V, 22K, .047μf
			CAP. SPRAGUE, TYPE 3CI5, 25V, 20K, .082μf
	CR1009		DIODE FAIRCHILD 1N3067
	CR1010		DIODE, 1N3067
	CR1011		DIODE, 1N3067
	CR1012		DIODE, 1N3067
	CR1013		DIODE, 1, 1N3067
	CR1014		DIODE FAIRCHILD, 1N751-A

GPS-5			1

DATA CONTROL SYSTEMS, INC.

PLUG-IN BOARD ASSY, D.C. RESTORER & LIMITER

C.N.	10/15/63	
1937	10-17-63	
	2-24-64	
2 X	5-29-64	

TA-011540 G

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-2824-SYMM. ADJUSTMENT	9/3/65	[illegible]	RWG	HM
C	CA-2768-1-DELETED NOTE 2	9/16/65	[illegible]	[illegible]	[illegible]
D	CA-3130 CHG'D COMPONENTS	3/29/66	[illegible]	[illegible]	[illegible]
E	CA-3180-2 CHG'D COMPONENTS	4/12/66	P.I.	[illegible]	[illegible]

BW-012856 REV. E

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY./ASSY.

C +24V

B +12V

A

DATA SYMMETRY
R1039
2K

R1041
15K

R1040
2.2K

FROM FCB
BD1100
J1100-10

J1000-8

Q1007
2N3906

J

R1043
10K

CR1009
IN3067

CR1010
IN3067

R1045
1.15K
1%

CR1011
IN3067

Q1009
2N3906

R1046
1.2K

C1018
.047μf
25V

CR1012
IN3067

CR1014
IN751A
5V

C1013
IN3067

D

J1000-10

DOUBLER CAP

IN TU

TO PHASE COMP. BD1700 J1100-14

$C(\mu f) = \frac{351.5}{fck}$

DATA FROM LIMITER

H

R1042
150Ω

Q1008
2N3391A

Q1010
2N3391A

R1044
1.1K
1%

R1048
150Ω

C1019
.047μf
25V

R1047
10Ω

G GRD

F -12V

E -24V

NOTES:
1) △ ELCO PIN CONNECTIONS ON LIMITER BD 1000 TO MOTHER BD1500
2) □ CONNECTIONS BETWEEN TA-011540 & LIMITER BD 1000 SERIES. REF SCHEMATIC TW-012723
3) ALL RESISTORS AB, CB 1/4W, 10% UNLESS OTHERWISE NOTED.

REF.	DESCRIPTION	QTY

GPS-5		
PRODUCT	NEXT ASSEMBLY	QTY./ASSY.

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC
DC Restorer and Limiter (Plug-in)

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0. + 1/64
NOTE- BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN. DH		1/19/65
CHKD. [illegible]		1/19/65
ENG. [illegible]		2/16/65
APP. [illegible]		2/16/65
SCALE ~		

DO NOT SCALE DRAWING
MAT'L ~
FINISH ~

BW-012856 REV. E

SHEET

	Q1104		TRANS, G.E.	2N3903A	1
	Q1105		FAIRCHILD	2N2222A	1
	Q1106		MOTOROLA	2N3906	1
	Q1107		MOTOROLA	2N2218	1
	Q1108		G.E	2N3904	1
	Q1109		MOTOROLA	2N3906	1
	Q1110		G.E	2N3251A	1
	Q1111			2N3906	1
	CR1101		DIODE G.E	1N914A	1
	CR1102		G.E	IN2941-A	1
	CR1103		TI	IN816	1
	CR1104			OMIT	1
	CR1105		FAIRCHILD	IN3600	1
	CR1106			IN3600	1
	CR1107		CONT DEVICES	IN1692A	1
	CR1108		CONT DEVICES	IN752A	1
	CR1109		CONT DEVICES	IN3064	1
	CR1110	SEE ITEM A	MOTOROLA	MR1503	1
	CR1111		TRANSITRON	IN456	1
	CR1112		CONT DEV.	IN3067	1
	CR1113		TRANSITRON	IN456	1
2			PAD, TRANS, MILTON ROY	#1	6
3				#1	6
4				#1	1

SIEMENS-ELEMA INTERNATIONAL

DWG NO.	INSIDE DIA.	INSIDE DIA.	LENGTH	MATERIAL
67E [illegible]	[illegible]	1.2 MM	[illegible]	[illegible]

ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
	R1136		RES, AB, CB, 1/4W, 10%	10K	1
	R1137			220Ω	1
	R1138			3.3K	1
	R1139		POT, CIRCUITRIM, IRC, 201-10	10K	1
	R1140		RES, AB, CB, 1/4W, 10%	100K	1
	R1141			47K	1
	R1142			220Ω	1
	R1143			390K	1
	R1144			1K	1
	R1145			1K	1
	R1146			220K	1
	R1147			220Ω	1
	R1148			4.7 MEG	1
	R1149		POT, IRC, CIRCUITRIM, 201-10	20K	1
	R1150		RES, AB, CB, 1/4W, 10%	10K	1
	C1101		CAP, ERIE, 831-000 X5F0-471K	470μμF	1
	C1102		SPRAGUE, 3C15, 25V, 20%	.047μF	1
	C1103		SPRAGUE, 3C15, 25V, 20%	.047μF	1
	C1104		ERIE 831X5R-680K	68μμF	1
	C1105		SPRAGUE 3C15, 25V, 20%	.047μF	1
	C1106		KEMET, K47P35, 10%	.47μF	1
	C1108		ERIE, 831X5R-680K	68μμF	1
	C1109		SPRAGUE, 3C15, 25V, 20%	.047μF	1
	C1110		SPRAGUE, 3C15, 25V, 20%	.047μF	1
	C1111		DURMICA, DM10, (FA)	2-10μμF	1
	C1112		ERIE, 851X5R-102K	1000μμF	1
	C1119		KEMET, K1P35, 20%, 35V	1.0μF	1
	C1120			1.0μF	1
	C1121			1.0μF	1
	C1122			1.0μF	1
	C1123			1.0μF	1
	C1124			1.0μF	1
	Q1101		TRANS, MOTOROLA	2N3906	1
	Q1102			2N3906	1
	Q1103			2N3906	1

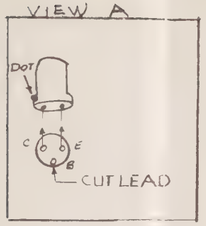
ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D
		CF-012550-A	BOARD, PC, [illegible]	1
	R1101		RES, AB, CB, 1/4W, 10%	4.7K	1
	R1102		T.I.	15K	1
	R1103		ELECTRA, MF5C-D, 1/4W, 1%	1.24K	1
	R1104		AB, CB, 1/4W, 10%	47K	1
	R1105		POT, IRC, CIRCUITRIM, [illegible]	[illegible]	1
	R1106		RES, AB, CB, 1/4W, 10%	[illegible]	1
	R1107			47Ω	1
	R1108			56	1
	R1109			1.8K	1
	R1110		ELECTRA, MF5C-D, 1/4W, 1%	3.01K	1
	R1111		AB, CB, 1/4W, 10%	5.6K	1
	R1112		ELECTRA, MF5C-D, 1/4W, 1%	31.6K	1
	R1113		AB, CB, 1/4W, 10%	100K	1
	R1114		AB, CB, 1/4W, 10%	18K	1
	R1115		POT, IRC, CIRCUITRIM, 201-10	10K	1
	R1116		RES, ELECTRA, MF5C-D, 1/4W, 1%	1.47K	1
	R1117			[illegible]	1
	R1118			86.6K	1
	R1119			[illegible]	1
	R1120			1.33K	1
	R1121		AB, CB, 1/4W, 10%	150Ω	1
	R1122			1K	1
	R1123			100Ω	1
	R1124		ELECTRA, MF5C-D, 1/4W, 1%	1.0K	1
	R1125		ELECTRA, MF5C-D, 1/4W, 1%	1.0K	1
	R1126		AB, CB, 1/4W, 10%	[illegible]	1
	R1127			15Ω	1
	R1128			150Ω	1
	R1129			15Ω	1
	R1130			150Ω	1
	R1131			1.5K	1
	R1132		ELECTRA, MF5C-D, 1/4W, 1%	3.16K	1
	R1133		ELECTRA, MF5C-D, 1/4W, 1%	3.16K	1
	R1134		AB, CB, 1/4W, 10%	3.3K	1
	R1135		AB, CB, 1/4W, 10%	3.3K	1

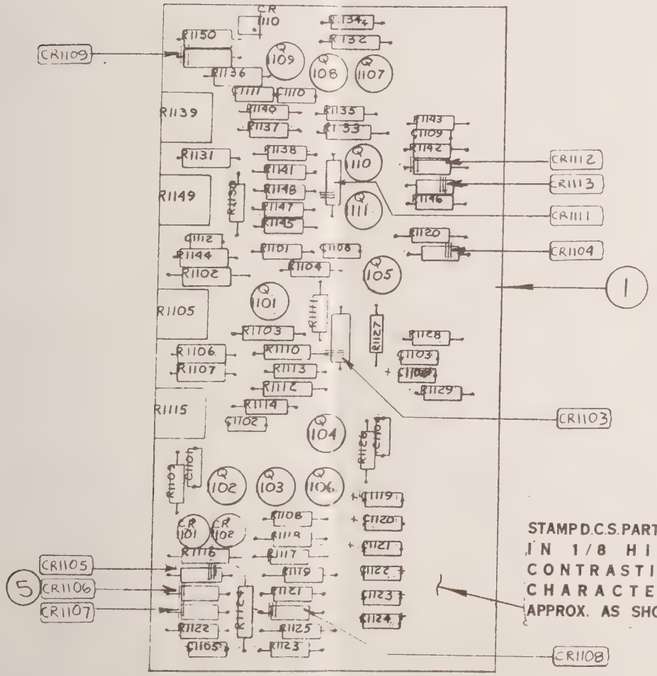
ITEM	SYMBOL	PART NO	DESCRIPTION	QTY REQ'D

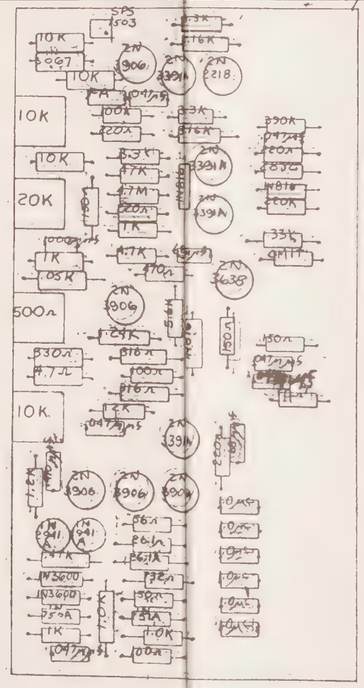
M	CA-4005 ADD NOTE #6	2/9/66	[illegible]	[illegible]	[illegible]
N	CA-4230 ADD ITEM # 5	2/9/66	[illegible]	[illegible]	[illegible]
P	CA-4263 CHG. R1138 FROM 6.8 TO 3.3K	2/9/66	[illegible]	[illegible]	[illegible]
R	CA-4230-1 MOVED ITEM 6 TO BALLOON 5	3-9-66	[illegible]	[illegible]	[illegible]

REVISIONS

SYM.	DESCRIPTION	DATE	BY	CHK'D	APP'D
D	(R&E) REDRAWN	3/9/66	WB		
E	CA-3190- CHG'D. COMPONENTS	3/10/66	P.I.		
F	CA-3190-1- CHG'D, R1105 TO 2N3638	3/23/66	P.I.		
G	CA-3317- CHG'D CR1112 TO 2BJ2	4/5/66	P.I.		
H	CA-3535- CHG'D CR1112 MFG.	1/9/67	P.I.		
J	CA-3849 CHG. CAP TYPE	7/11/67	[illegible]		
K	CA-3881 ADD C1107.	9/14/67	[illegible]		
L	CA-3881-1 REMOVED ALL CHANGES PER CA-3881	10/26/67	[illegible]		







NOTES:

1) INSTALL ITEM 2 UNDER Q1101, Q1102, Q1103, Q1105, Q1106
2) INSTALL ITEM 3 UNDER Q1104, Q1107, Q1108, Q1109, Q1110, Q1111
3) ADD TRANSPARENT SLEEVING TO COMPONENTS HAVING COPPER UNDERNEATH ON COMPONENT SIDE.
4) ALL AB, CB, 1/4W, 10% RESISTOR TO CONFORM TO MS 35350.
5) INSTALL ITEM 4 UNDER R1115, R1105, R1149, R1139
6) Q1105 TO USE 2N3638 ONLY; NO SECOND CHOICE.

DATA CONTROL SYSTEMS, INC.

TITLE: BD. ASSY, V.C.O. GP3-5

TOLERANCES: UNLESS OTHERWISE SPECIFIED		DATE	DO NOT SCALE DRAWING
DECIMAL - 3 PLACE ± .005	DWN. WB	3/9/66	
DECIMAL - 2 PLACE ± .010	CHKD. [illegible]	3-10-66	MAT'L
FRAC. ± 1/64 ANG. ± 0°30'	PROJ. ENG. BT	3-14-66	FINISH
FLATNESS WITHIN /IN.	CH. ENG. [illegible]	3/14/66	
FRACTIONAL HOLES -0, + 1/64			GA-011734 REV D
NOTE: BREAK ALL SHARP CORNERS .005 - .015			

REV	DESCRIPTION	DATE	DWN	CHK	APP
B	CA-2829 ADDED C1119 C1120 & C1121	4/14/65	RB	CWS	HM
C	CA-2829 - CHG'D R1145 PER CA	5/14/65	RB		
D	CA-3190 - CHG'D COMPONENTS	2/28/66	DI		
E	CA-3190-1 - CHG'D. Q1105	3/23/66	DI		
F	CA-3317 - CHG'D CR1112 FR 1N811	9/5/66	DI		
G	[illegible]	1/16/67	DI		
H	[illegible]	8/[illegible]			
J	[illegible]	[illegible]			
K	CA-4005 REV NOTE *6	2/16/68	DI	MP	MR
L	CA-4263 CHG R1138 FROM 7.5K TO 33K	2/14/69	DI	MP	DF

REF	DESCRIPTION	QTY

TW-012496 L

ITEM	SYMBOL	DWG NO	DESCRIPTION	QTY ASSY

NOTES:
1. ○ TERMINALS ON VCO DC AMP BD
2. □ TERMINALS ON PHASE COMPARATOR BD
3. REF ASSY TA-01734
4. BLOCK DIAGRAM DB-01331Z
5. △ ELCO CONNECTION TO MOTHER BD 1500
*Q1105 TO USE 2N3638 FOR 1.0 SECOND [illegible]

+24V J1100-1
+12V J1100-2
+8V J1100-3
-8V J1100-4
-12V J1100-5
-24V J1100-6
GRD J1100-7
J1100-8
J1100-9
J1100-10
J1100-11
J1100-12
J1100-13

C1119 1.0μf
C1120 1.0μf
C1121 1.0μf
C1106 .47μf
C1101 470μμf
C1102 .047μf
C1103 .047μf
C1105 .047μf
C1107 68μμf
C1108 68μμf
C1109 68μμf
C1110 .047μf
C1111 2Nμμf NOM
C1112 1000μμf

R1101 4.7K
R1102 1.05K 1/2W
R1103 1.24K
R1104 470Ω
R1105 500Ω VCO FREQ RANGE
R1106 330Ω
R1107 47Ω
R1108 56Ω
R1109 1.2K
R1110 316Ω
R1111 5.6K
R1112 316Ω
R1113 100Ω
R1114 12K
R1115 10K VCO SYM
R1116 1.47K
R1117 26.1Ω
R1118 26.1Ω
R1119 732Ω VCO TIMING CAP INT.U.
R1120 1.33K
R1121 150Ω
R1122 1K
R1123 100Ω
R1124 1.0K
R1125 1.0K
R1126 220Ω
R1127 150Ω
R1128 150Ω
R1129 10Ω
R1130 150Ω
R1131 10K
R1132 GPS-1503 3.16K
R1133 3.16K
R1134 3.3K
R1135 3.3K
R1136 10K
R1137 220Ω
R1138 3.3K
R1139 10K FCB ZERO ADJ
R1140 100K
R1141 47K
R1142 220Ω
R1143 390K
R1145 1K
R1146 220K
R1147 220Ω
R1148 4.7MEG
R1149 20K PHASE COMP. ZERO

Q1101 2N3906
Q1102 2N3906
Q1103 2N3906
Q1104 2N3906
Q1105 2N3638 *
Q1106 2N3906
Q1107 2N2218
Q1108 2N3638 A
Q1109 2N3906
Q1110 2N3391A
Q1111 2N3391A
Q1109 2N3391A

CR1102 1N2991A
CR1103 1N816
CR1105 1N3600
CR1106 1N3600
CR1107 1N750A
CR1108 1N751A
CR1109 1N3067
CR1110 GPS-1503
CR1111 1N816
CR1112 1N3067
CR1113 1N816

TP1101 FCB

OPERATE
SET
100Ω
FROM PHASE COMP BD-1700
MODE SWITCH ON CONTROL UNIT
LOOP FILTER IN T.U.
TO PHASE COMP BD-1700
FCB J1100-10
TO INTEG. & DOUBLER
FREQ ADJ IN T.U.
-12V
-24V
TO VCO QUAD CIRCUIT BD-1700
TO METER AMP BD-1700
TO VCO DRIVERS J1100-11 BD-1200

R1115 R1105 R1149 R1139 TP1101
1 2 3
SKETCH SHOWING LOCATION & IDENTIFICATION OF TERMINALS & TEST POINTS.

GPS-5
FIRST PRODUCT
NEXT ASSEMBLY
REF
QTY ASSY

DATA CONTROL SYSTEMS, INC.

TITLE: SCHEMATIC, VCO, DC AMP

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL 3 PLACE ± .005
DECIMAL 2 PLACE ± .010
FRAC ± 1/64 ANG ± 0°30'
FLATNESS WITHIN ~ /in.
FRACTIONAL HOLES Ø + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015" SURFACE ROUGHNESS NOT TO EXCEED ~

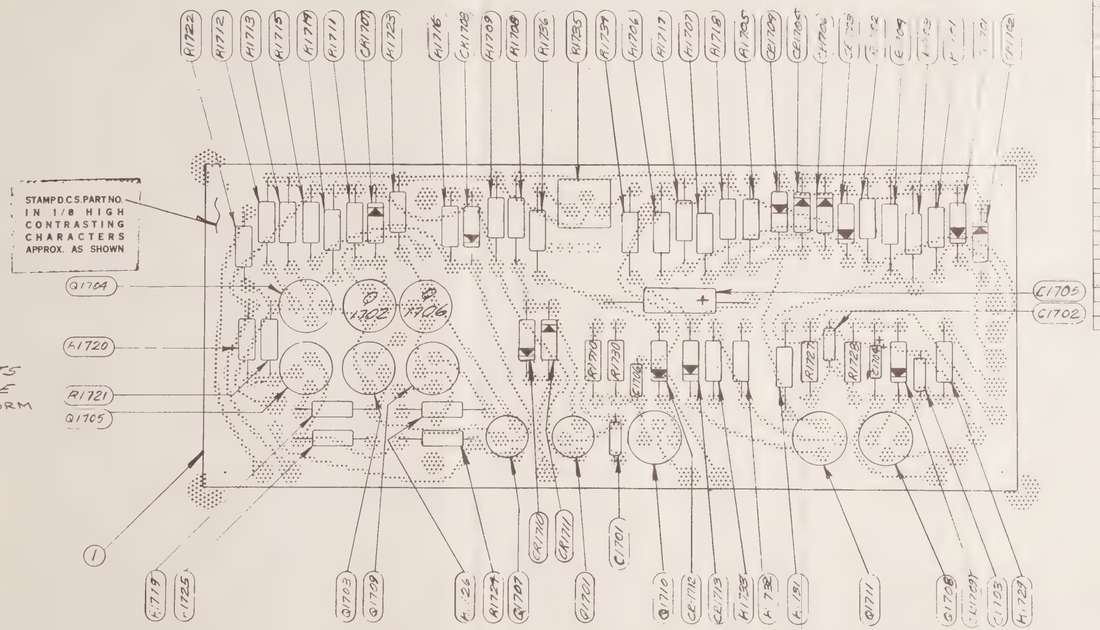
		DATE
DWN	DH	1/14/65
CHKD		
ENG.		
APP.		
SCALE	2	

DO NOT SCALE DRAWING
MAT'L
FINISH

TW-012496 REV. L

SHEET

REV	DESCRIPTION	DATE	DWN	CHK	APP
B	CA-3130-CHGD COMPONENTS	7/28/66	[illegible]	[illegible]	[illegible]
C	CA-3849 CHGD CAP VALUES	9/11/67	[illegible]	[illegible]	[illegible]



1. ADD TRANSPARENT SLEEVING TO COMPONENTS HAVING COPPER UNDERNEATH ON COMPONENT SIDE
2. ALL ALLEN BRADLEY CB, 1/4W, 10% RESISTORS TO CONFORM TO MS 35350

TA-012105 REV C

	C1705	CAP, CER, ERIE, 8131-000-X5F0-471K, 470PF		
	Q1708	TRANS, MOTOROLA 2N2219A		
	Q1701	TRANS, GE [illegible]		
	R1725	[illegible]		
	R1702	[illegible]		
	R1703	[illegible]		
	R1705	[illegible]		
	R1706	[illegible]		
	R1707	[illegible]		
	R1708	[illegible]		
	S1701	[illegible]		
2		PAD, TRANS, MOTOROLA A10068	10	
	CR1701	DIODE, TRANSISTOR, 5266G		
	CR1702	5266G		
	CR1703	5266G		
	C1704	[illegible]		
	CR1705	[illegible]		
	CR1706	[illegible]		
	R1727	[illegible]		
	R1728	[illegible]		
	CR1709	[illegible]		
	CR1710	DIODE, SILICON, [illegible]		
	CR1711	[illegible]		
	CR1712	[illegible]		
	CR1713	[illegible]		

NOTE.
1. * NOMINAL VALUE 390K
2. INSTALL ITEM 2 UNDER Q1701 THRU & INCLUDING Q1711

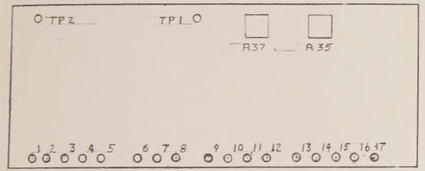
ITEM	SYMBOL	DWG NO	DESCRIPTION	QTY
		CF-012442-3	PC, FAB, [illegible]	1
	R1701		RES, [illegible]	
	R1702			
	R1705			
	R1706			
	R1707			
	R1708			
	R1709			
	R1712			
	R1713			
	R1714			
	R1717			
	R1718			
	R1731			
	R1734			
	R1736			
*	R1703			
*	[illegible]			
	[illegible]			
	[illegible]			

REV.	DESCRIPTION	DATE	DWN.	CHK.	APP.
B	CA-3982 ADD NOTE #1	11/1/67	[illegible]	[illegible]	[illegible]
C	CA-4413 CHG'D COMP. SERIES	4-9-68	[illegible]	BR	BR

TW-015280

ITEM	SYMBOL	DWG. NO.	DESCRIPTION	QTY/ASSY

Ø METER VCO QUAD.
DOUBLER FCB ZERO SYMMETRY



SKETCH SHOWING LOCATION & IDENTIFICATION OF TERMINALS & TEST POINTS.

NOTES:
* 1) -1 DESIGNATES THE USE OF CR-9 & CR10
-2 " OMISSION OF CR9 & THE REPLACEMENT OF CR10 WITH #22 BUSS JUMP.

2. △ ELCO PIN CONN ON VCO BD1100 TO MOTHER BD
3. O TERMINALS ON VCO BD
4. REF. ASSY GA-015155
5. REF. BLOCK DIAGRAM DB-015327
6. O TERMINAL ON Ø COMP BD
7. RESISTORS ARE AB, CB, 1/4W, 10% UNLESS OTHERWISE NOTED.

8) -1 INDICATES GPS-5&6
-2 " " GPD-6

J1100-1 △ 1 +24V
J1100-3 △ 17 +8V
J1100-17 △ 1
16 TO SET/OPR. MTR. CKT
13 FROM VCO
J1100-18 △ 12 THRU FRONT PANEL MODE SW. TO DC AMP INPUT
TP1701 Ø COMP FCB
3 ○ 9 FROM DC AMP
J1100-16 △ 7 FROM POTTED MODULE THRU T.U. CAP
J1100-20 △ 3 LOCK OUT
J1100-2 △ 4 +12V
J1100-5 △ 2 -12V
J1100-6 △ 8 -24V
J1100-7 △ 5 GRD
J1100-8 △ 15 -8V
2 ○ 14 FROM VCO
11 ○ J1100-11 TO Ø METER
J1100-13 △ 10 TO Ø METER
6 ○ J1100-19 TO SET/OPR. METER CIRCUIT
DOUBLER TP-2

R-1 121K 1%
R-2 121K 1%
R-3 382K 1%
R-4 382K 1%
R-5 215Ω 1%
R-6 215Ω 1%
R-7 215Ω 1%
R-8 1.96K 1% 1/2W
R-9 1.05K 1%
R-10 68Ω
R-11 560Ω
R-12 825Ω 1%
R-13 2.37K 1%
R-14 1.0K 1%
R-15 560Ω
R-16 22K
R-17 6.81K 1%
R-18 6.81K 1%
R-19 1K
R-20 12K
R-21 2.2K
R-22 8.2K
R-23 3.3K
R-24 470Ω
R-25 1.5K
R-26 2.2K
R-27 150Ω
R-28 1K
R-29 150Ω
R-30 1K
R-31 4.22K 1%
R-32 5.6K
R-33 300Ω
R-34 2.61K 1%
R-35 1K
R-36 2.61K 1%
R-37 20K
R-38 5.6K
R-39 470Ω
R-40 1.5K
R-41 1.2K
C-1 .047μf
C-2 .047μf
C-3 .047μf
C-4 4.7μf 10V
C-5 680pf
C-6 470pf
C7 470pf
C8 FCB 1-10pf
CR-1 IN993
CR-2 IN993
CR-3 IN993
CR-4 IN993
CR-5 IN993
CR-6 IN993
CR-7 IN3067
CR-8 IN3067
CR-9 * IN3067
CR-10 * IN3067
CR11 CGD1032
CR12
Q-1 TN53 or 2N2218
Q-2 2N3906
Q-3 2N3906
Q-4 2N4250
Q-5 2N3391A
Q-6 2N3906
Q-7 2N3906
Q-8 2N3638
Q-9 TN53 or 2N2218
Q10 2N3906
Q-11 2N3906

REF	DESCRIPTION	QTY

GPS-5&6
GPD-6
FIRST PRODUCT | NEXT ASSEMBLY | QTY/ASSY

1700 SERIES

DATA CONTROL SYSTEMS, INC.

TITLE SCHEMATIC, PHASE COMPARATOR

DO NOT SCALE DRAWING

TOLERANCES: UNLESS OTHERWISE SPECIFIED
DECIMAL - 3 PLACE ± .005
DECIMAL - 2 PLACE ± .010
FRAC. ± 1/64 ANG. ± 0°30'
FLATNESS WITHIN ~ /IN.
FRACTIONAL HOLES -0 + 1/64
NOTE: BREAK ALL SHARP CORNERS .005"-.015"
SURFACE ROUGHNESS NOT TO EXCEED ~

		DATE
DWN.	C.C.G.	10/28/66
CHK'D	BR	4/9/67
ENG.	K.M.M.	4/17/67
APP.	BR	4/19/67
SCALE		FINISH

MAT'L

TW-015280 REV. C

SHEET